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*Jupiter Europa Orbiter Mission*

# Designing Circuits and Systems for Single-Event Effects

**Prepared by**

**Allan H. Johnston**
**Jet Propulsion Laboratory**
**4800 Oak Grove Drive**
**Pasadena, CA 91109**

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**Jet Propulsion Laboratory**
**California Institute of Technology**
**Pasadena, California**

# Designing Circuits and Systems for Single-Event Effects

Outline

1 Introduction
- Basic Considerations
- Control Plan for SEE Effects on Europa

II SEU and Related Effects: Non-Catastrophic Phenomena
- Single-event upset (SEU)
- More complex SEU effects
- Summary of effects related to simple SEU

III Detectors
- Basic issues
- Photodiodes and related devices
- CCDs and active pixel sensors

IV Environments
- Galactic cosmic rays
- Solar flares
- High energy protons

V Catastrophic SEE Effects
- Stuck bits
- Latchup (SEL)
- Gate rupture (SEGR)
- Single-event burnout (SEB)

VI SEE Testing Concerns
- Basic issues
- Statistical concerns
- Data interpretation

VII Qualifying Devices for SEE Effects
- Device variability

VIII General Recommendations and Requirements

IX. Summary and Conclusions

# Designing Circuits and Systems for SEE Effects

## I. Introduction

*A. Basic Considerations*

Single-event effects (SEE) on semiconductor devices in space were first discovered on an operational spacecraft in 1975, a surprising result that started a new sub-discipline in radiation effects. The rapid changes in microcircuit technology that have occurred within the last 40 years and the limited understanding of SEE effects and mechanisms when they were first discovered has increased the difficulty of dealing with these effects in space systems. As feature sizes have decreased, semiconductor devices have generally become more sensitive to this environment. Several new SEE phenomena have been discovered along the way, and these new effects have to be dealt with along with the "simple" single upsets that were first encountered in 1975.

It is important to realize that SEE effects are the result of the interaction of one energetic particle, in contrast to total dose and displacement damage which are the integrated effect of the interaction of a large number of particles. All single-event effects are statistical in nature, and we have to incorporate the statistics of the environment and the probability that a particle strikes the (small) sensitive region of a specific device when we estimate the effects of SEE interactions. The best we can do is to calculate a probability for such events. A basic understanding of statistical concepts is essential in dealing with all SEE phenomena.

Even though SEE effects are extremely important, JPL has never developed a guideline or tutorial document on how to deal with them. The Institutional Parts and Program Requirements document (IPPR) states the end requirements, but provides little information beyond that. For example, there are three conditions for SEU within the IPPR:

1. No observed upsets when a part is tested to an LET of 75 MeV-cm$^2$/mg, or
2. Verification of an SEU rate < $10^{-10}$ upsets per bit day, or
3. Calculation of a device upset rate that is less than the required circuit upset rate as determined by circuit SEU analysis.

No information is provided as to how the conditions were established, or how such requirements affect either component qualification or the design of circuits and systems. However, from Condition (3) it is clear that the ultimate determination of how such effects should be dealt with depends on the application. For this reason there is a much more direct connection between a specific circuit application and SEE sensitivity than for total dose and displacement damage effects.

There are additional requirements for other SEE effects that will be discussed later, including some that can cause permanent damage, not just temporary malfunctions.

The purpose of this document is to provide more specific information about SEE, along with examples of ways to deal with them. In many cases the significance of an SEE event is application dependent, increasing the difficulty of dealing with SEE from a parts specification standpoint. Nevertheless, part specifications and testing methods are vital in this process because we need valid data and models in order to calculate the upset rate, the necessary starting point.

In the first part of the introduction to this document we will discuss SEE phenomena in some detail, noting the specific device technologies where the effects are important as well as whether the effects are temporary in nature, or can produce permanent damage.

Galactic cosmic rays in space are the main cause of SEE in spacecraft (except those in low-earth orbit). Cosmic rays are extremely energetic, producing a short-duration pulse of electron-hole pairs when they interact with a semiconductor or insulator. The unit used to describe the ionization "strength" of a galactic cosmic ray is ***linear energy transfer*** (LET), with units of MeV-cm$^2$/mg. A more intuitive approach for semiconductor devices is to express the ionization charge that is deposited per path length. For silicon, the relationship between LET and specific charge deposition is

$$\text{LET}^{*}\ (\text{in pC}/\mu\text{m}) \;=\; 0.0104\ \text{LET}\ \ (\text{in MeV}-\text{cm}^2/\text{mg}) \qquad (1)$$

Thus, a particle with an LET of 100 MeV-cm$^2$/mg, which is about the highest value we have to be concerned with, will deposit about 1.04 pC of charge in each micron of path length that it traverses within silicon.

The actual amount of charge that is collected depends on the path length within the device where charge can be collected by a semiconductor junction, along with the angle of incidence of the incoming particle. Most microelectronic devices have a wide aspect ratio (shallow depth, with relatively long surface dimensions. For such a geometry, a particle strike at an oblique angle will have a longer path length compared to a particle at normal incidence. The net amount of deposited charge will increase as $1/\cos(\theta)$, where $\theta$ is the angle of incidence. Fig. 1 shows a simple diagram. This concept is very important, because energetic particles in space – which are omni-directional - will deposit considerably more charge in the thin collection regions that are typical of most semiconductor devices than implied by the LET value when it is applied to the junction depth at normal incidence.

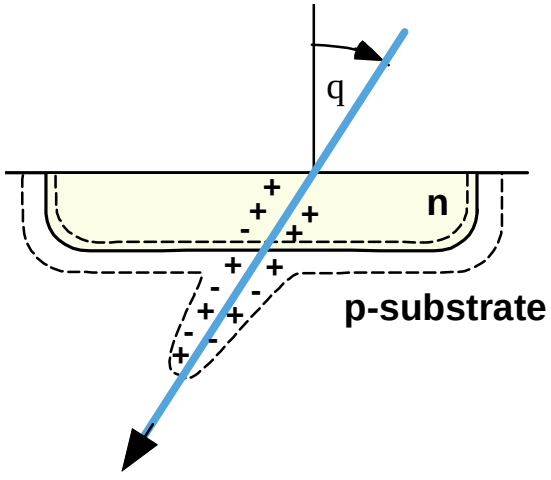


Fig. 1. Diagram showing the increase path length of a long-range ion that strikes a semiconductor p-n junction at an angle. The amount of charge deposited by the particle increases by a factor1/cos(θ).

We shall return to this later in the discussion of SEE environments in Section III.

*B. Control Plan for SEE Effects on the Europa Orbiter*

As discussed in later sections of this document, a variety of effects can be produced in microelectronic and optoelectronic devices by heavy ions and energetic protons in space. Some of these effects, such as latchup, are catastrophic (or potentially catastrophic), and must be dealt with in a thorough, careful manner in order to avoid compromising the operation of the spacecraft or its instruments during the mission. Other effects are transient in nature, causing an internal disruption in storage elements or of the fundamental operation of the device. "Simple" upsets can often be dealt with in a straightforward manner, but very complex upset signatures can occur in complex devices that are more difficult to deal with.

In general SEU effects have become worse with scaling, partly because less charge is required to produce upsets in scaled devices, and also because the total number of active transistors within a circuit often increases with scaling, particular for high-performance digital parts, such as microprocessors and memories..

SEU effects can vary due to deliberate changes by the manufacturer that are introduced to increase yield and performance. Consequently it is essential that SEU effects are evaluated for the specific devices that are used in the Europa Orbiter. ***Although older data on specific part types may be a useful guide for the initial selection of components for the mission, the general requirement for Europa is that test data must be obtained on parts from the flight lot***. An exception can be made for radiation-hardened devices that are specifically designed to meet SEE requirements.

There are many different types of SEE, some of which are related to device complexity. These effects will be discussed in some detail later in the guideline. An overview and definition of SEE acronyms is shown in Table 1.

Table 1. Overview of SEE Effects and Acronyms

| Phenomenon | Acronym | Basic Characteristics | Comments |
|---|---|---|---|
| Single-event upset | SEU | Transient, but circuit recovery may require extra steps | |
| Single-event latchup | SEL | Potentially catastrophic | Highly temperature sensitive |
| Single-event transient | SET | Transient | |
| Single-event gate rupture | SEGR | Catastrophic | Only affects power MOSFETs |
| Single-event burnout | SEB | Catastrophic | Only affects power MOSFETS and bipolar power transistors |

Fortunately many of these effects are confined to relatively few part technologies, as shown in Table 2. This simplifies the overall problem of dealing with SEE, and also reduces the number of effects that have to be dealt with from the standpoint of testing and qualification.

Table 2. Susceptibility of Various Part Types to SEE Effects

| Part Technology | Protons | Heavy Ions | | | | Comments |
|---|---|---|---|---|---|---|
| | | SEU | Latchup | SEGR | SEB | |
| Digital Logic | | | | | | |
| CMOS | | X | X | | | SEL not required for SOI |
| Bipolar | | X | | | | |
| Memory | | X | X | | | |
| Linear | | | | | | |
| CMOS | | X | X | | | |
| Bipolar | X | X | | | | |
| Mixed Signal | | | | | | |
| CMOS | | X | X | | | |
| BiCMOS | | X | X | | | |
| Bipolar | X | X | | | | |
| Power Transistors | | | | | X | |
| Power MOSFETs | | | | X | X | |
| Power Circuits | | X | X | X | X | Assumes power MOSFETs |
| Hybrid devices | | X | X | X | X | Assumes power MOSFETs |
| Optoelectronics | | | | | | |
| Detectors | X | X | | | | |
| Optical Emitters | | | | | | |
| Circuits, subsys. | X | X | X | | | |

The control plan for Europa requires SEE testing of most parts that are sensitive – or potentially sensitive – to SEE. Testing must be done under conditions that approximate actual use conditions. The detailed requirements for testing and evaluation of test results are discussed in a later section.

*C. Mitigation Methods*

Ideally parts would be selected that are immune from SEE, a tremendous simplification. This is sometimes possible by using special SEE-hardened circuits. However, hardening often implies a much lower event rate, not complete relief from SEE effects. It is usually necessary to take upset rates into account even for hardened devices when they are used in a complex, high-value mission such as Europa.

A number of approaches have been developed to deal with SEE effects. Many circuit and system techniques have been developed for this purpose, including

- Use of clocked circuits that reduce vulnerability to the short transition time related to the clock
- Redundancy
- Adding capacitive loading to reduce circuit response time beyond the short-term duration of the pulse associated with the SEU
- Error detection and circumvention (EDAC) [ *which is really a system solution, although it can be incorporated within individual circuits*]
- Watchdog timers that provide a periodic signal verifying normal operation

- Parity checking (along with associated system corrections when parity errors occur)
- Triple-redundancy with majority voting

Special mitigation methods have also been developed for latchup, a potentially destructive effect in many CMOS circuits. However, latchup mitigation is strongly discouraged because of the difficulty of verifying its effectiveness.

A brief summary of mitigation strategies for various SEE phenomena is shown in Table 3. Note that part derating is an effective way to avoid SEGR and SEB in power devices. Part derating is normally included in tables showing acceptable design values that includes the extra derating required to avoid those two effects.

Table 3. Summary of Mitigation Approaches for SEE Phenomena

| Phenomenon | Mitigation Approach | Comments |
|---|---|---|
| Single-event upset | Circuit design, including clocked logic and redundancy | |
| Single-event latchup | None recommended | Elimination of latchup-prone devices is the recommended approach |
| Single-event transient | Circuit design that can tolerate occasional transients | |
| Single-event gate rupture | Derate drain and gate voltage | This is really avoidance rather than mitigation |
| Single-event burnout | Derate drain-source (or collector-emitter) voltage | |

## II. SEU and Related Effects: Non-Catastrophic Phenomena

### *A. Basic Single-Event Upset*

**SEU**. The basic concept of single-event upset (SEU) is relatively straightforward. If the spurious charge from a single energetic particle in space is sufficiently high, it can cause a basic storage element to flip to the opposite logic state, producing a logic error. The false state will remain until the circuit is re-initialized, but no permanent damage takes place. Fig. 2 shows a simple SRAM cell, where a bit flip can occur if the ion strikes either of two sensitive locations. Upset only takes place if the charge collected from an ion strike exceeds the critical charge for the circuit ($Q_c$). Furthermore the particle has to strike one of the sensitive regions – or sufficiently near one of them – in order to cause an upset to take place.

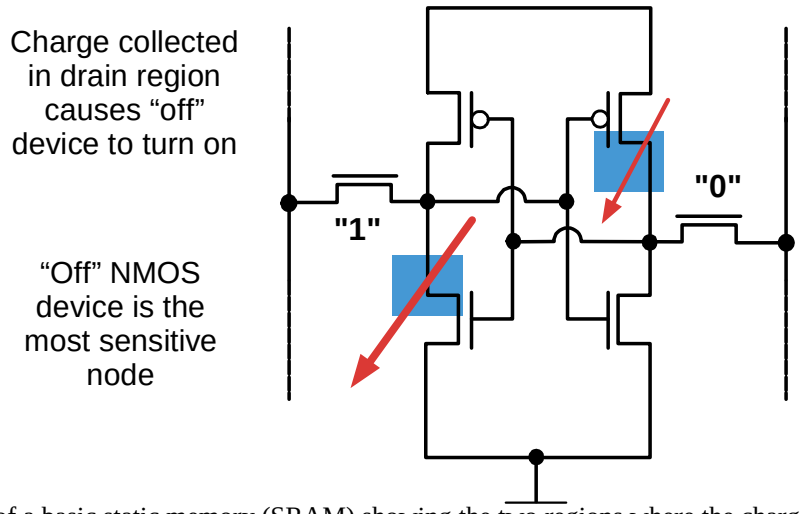


Fig. 2. Diagram of a basic static memory (SRAM) showing the two regions where the charge from an ion strike can cause the memory cell to change state.

The usual way of presenting information about SEU sensitivity is to plot the cross section – a measured quantity, related to the sensitive volume discussed above – versus linear energy transfer (LET), which, as discussed earlier, is effectively the ionization strength of an energetic charged particle in space. Fig. 3 shows an example of such data for a commercial memory along with a special radiation-hardened memory. In general the cross section increases for particles with higher LETs, and we can define two characteristics: the threshold LET, which is the lowest LET that can cause upset to occur; and a saturation cross section, which is the cross section where the curve flattens at high LET. (The relationship between particle LET and the radiation environment will be discussed in more detail in Section IV). The cross section can either be expressed in upsets per bit (often used for simple SEU effects), or in upsets per chip, which is appropriate for malfunctions that affect large regions within the device. This distinction must be carefully noted when SEU data are evaluated.

The occurrence of an upset does not necessarily cause a severe system effect, and there are several ways to deal with SEUs from a circuit or system standpoint. SEU effects can often be dealt with by using error-detection-and-correction (EDAC), which extends the word length to include extra parity bits. Various implementations are possible, but a commonly used approach is that of detecting and correcting single upsets within a word, but detecting multiple bit upsets without correction. For a 32-bit word this can be implemented by adding 7 additional parity bits.

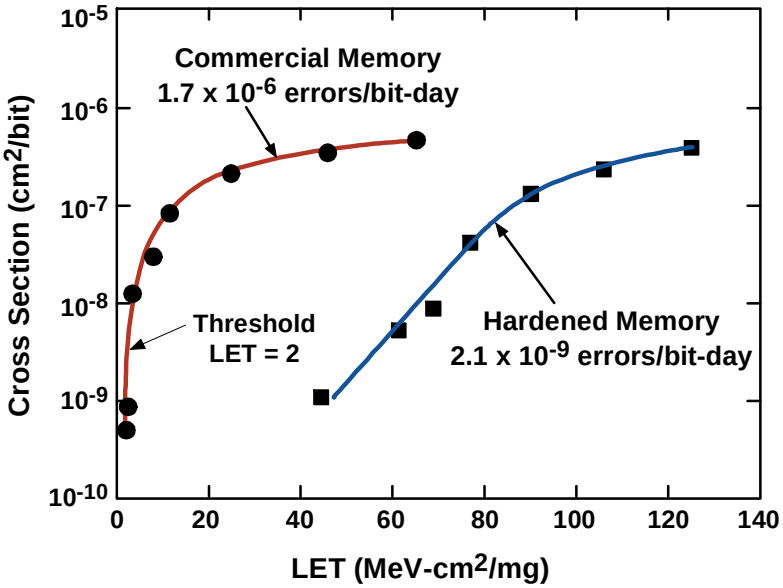


Fig. 3. Plot showing how the cross section for upset in a memory increases with particle LET. The data are obtained experimentally at a particle accelerator. The device lid must be removed for such tests because the particles available at most accelerators have much lower energy than particles in space, and are stopped by the package lid.

### *B. More Complex SEU Effects*

**MBU**. The first "extension" of a basic SEU is that of a multiple-bit upset (MBU), where a single particle strike produces a localized cluster of upsets instead of a single upset. Fig. 4. shows an example for an older 4-Mb DRAM where the mean number of upsets per event exceeds 2 for LET values > 20 MeV-cm$^2$/mg. As memories have scaled to smaller feature size, larger error clusters can occur.

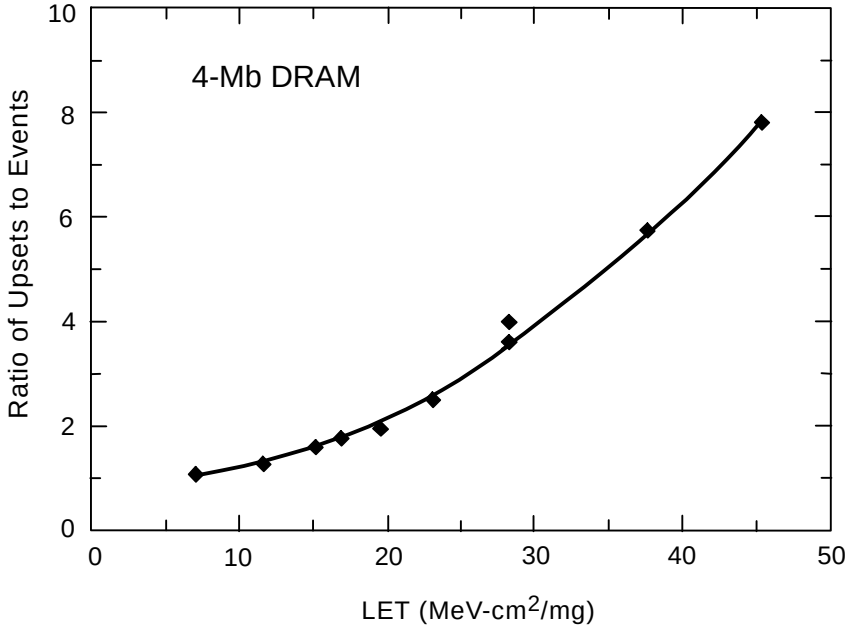


Fig. 4. Ratio of observed upsets to events vs. LET for a 4-Mb DRAM. On average several upsets take place for each event. Even larger numbers of MBUs can occur for more advanced memories.

More advanced error detection methods can be used to deal with MBUs. The most important factor is to recognize that they occur in large numbers, and that using simple EDAC methods will be only partially successful in mitigating these types of events unless the individual word bits are located in separate chips. Even with that option, one must be concerned about multiple errors within a word during the presence of an intense solar flare, which can increase the SEU rate by up to four orders of magnitude compared to the average rate from galactic cosmic rays.

**SEFI**. Another variant of an SEU is referred to as single-event functional interrupt (SEFI). Despite the awkward nomenclature, a SEFI effect is a basic SEU that happens to take place in a control bit where it alters the basic way in which the device responds to electrical signals because of the particular architecture of the circuit. A simple example is an internal test-mode flip-flop within a memory circuit, used by manufacturers to expedite testing at the wafer level. If such a flip-flop is triggered by an SEU, the memory will enter an abnormal operating mode that can cause extended regions to be erroneously written if the memory remains in such a condition.

SEFI effects have increased in importance as microcircuits have become more complex. Any circuit with complex internal architecture (such as a "state machine") is susceptible to SEFI effects. Advanced memories (including SDRAMs and flash memories) contain such architectures, as well as microprocessors and micro-controllers.

Fig. 5 shows an example for a more advanced memory, where about 0.01% of the total number of errors are SEFI events. The "SEFIs" occur in such large numbers that they will overwhelm conventional EDAC methods when they occur because they remain in place until the *entire chip* is re-initialized. SEFI events sometimes requires complete power removal in order to clear the condition.

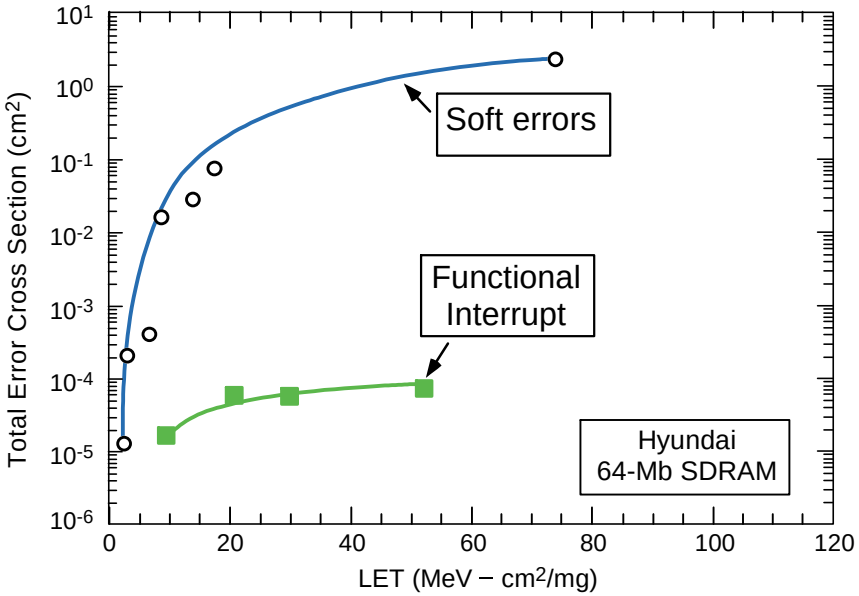


Fig. 5. Comparison of functional interrupt and soft error cross section for a 64-Mb SDRAM. A sizeable fraction of the events are SEFI events, which produce complex error signatures that cannot be handled with conventional EDAC.

SEFI events are even more important for microprocessors. Fig. 6 shows the cross section for two types of errors that cause the processor to "hang." The majority can be handled by re-initializing the processor, an involved procedure. About 0.02% of such events require that power is removed, with a complete re-start in order to clear the abnormal operating mode. This is a good illustration of just how severe SEFI effects can be for complex circuits.

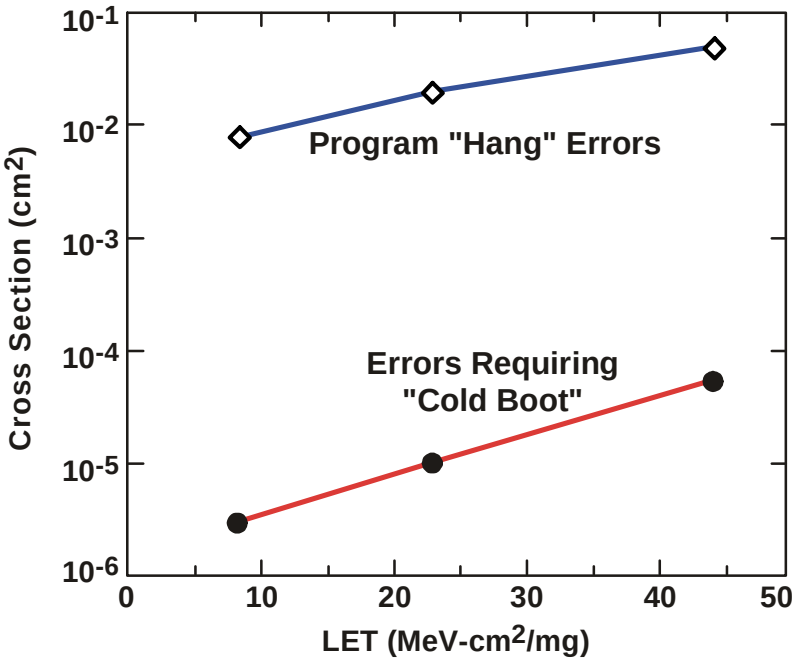


Fig. 6. Two types of SEFI events that were observed in tests of a 486 microprocessor. Although most of the events can be cleared by applying a reset signal followed by reiniitialization, about 0.1% of the events require power removal in order to restore operation.

**SET**. The last non-catastrophic SEE phenomenon is that of single-event transients (SETs). An SET is a transient pulse that can appear either at the output, or internally within a circuit. If the pulse has sufficient amplitude and duration, it can cause effects in other circuits (for a pulse at the output), or within a logic train for internal SETs. Fig. 7 shows experimental results for a comparator, tested with a single ion beam species (only one LET value). Transients observed during the experiment have a variety of amplitudes and pulse widths, depending on just where ions from the accelerator strike the device. If the amplitude and duration are large enough, the false signal generated at the output may affect circuits that are connected to the output.

SETs are particularly difficult to deal with because their properties are strongly affected by the circuit conditions that are used to evaluate the effect. For example, Aerospace data that was available for the LM139 comparator indicated that no transients should occur in an application of the LM139 within power converters, used on the Cassini spacecraft. Later tests done by JPL that more closely approximated actual use conditions showed that transients were expected (they were also observed during the mission). The Aerospace data was not incorrect, but it did not encompass the actual circuit conditions used on the Cassini application.

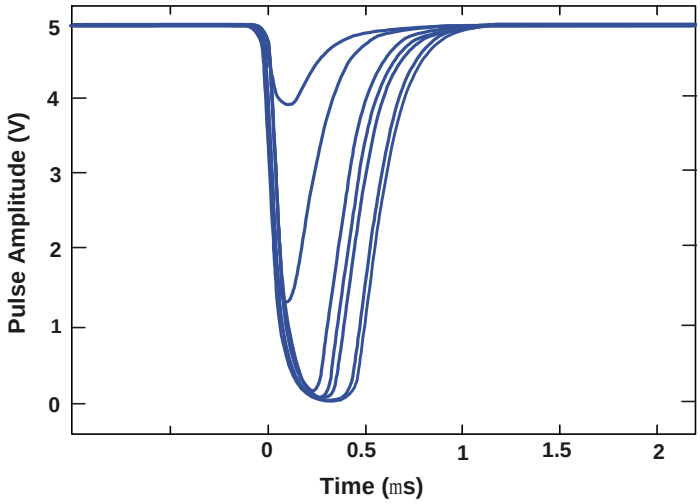


Fig. 7. Output pulses observed during tests of an LM139 comparator when a single ion species (one LET value) was used. The output transient varies, depending on where the ions happen to strike the device.

SETs can occur in voltage regulators as well as in comparators and operational amplifiers. SETs in regulators are particularly important because they can cause the output voltage to increase well above the expected output voltage. Even though the high voltage condition may only persist for tens of microseconds, it may destroy downstream circuits that are powered by the regulator.

### *C. Summary of Effects Related to Simple SEU*

Table 4 summarizes the various SEU effects that were discussed in this section. Even though none of them cause permanent effects, they can cause serious disruptions in operating spacecraft. MBU and SEFI effects are clearly more difficult to deal with.

Table 4. Summary of Non-Catastrophic SEE Phenomena

| **Effect** | **Circuit Technologies** | **Mitigation** |
|---|---|---|
| **SEU** | Any digital technology with internal storage elements | Simple error detection and correction. |
| **MBU** | Any digital technology with internal storage elements | Detection and correction of multiple errors. |
| **SEFI** | Any technology with internal storage elements that affect overall functional operation | Complicated. Depends on identifying the effect. May require power removal for recovery. |
| **SET** | Digital and analog circuits | Design of clocked circuits (digital)<br>Adding RC loads (analog) |

However, even simple effects such as SETs can have important effects. SETs in comparators that are used in power control modules on Cassini have exhibited about 25 “trip” events since 1997 that cause the power control module to either enter an un-commanded standby mode, or in some cases to trip from “on” to “off”. Fortunately the event rate is low enough to avoid serious operational problems, but this could have been a very difficult issue if the designers had used a lower threshold condition for the comparator application because the event rate could be high enough to cause such trips on a weekly basis.

Fundamentally it is much easier to deal with these types of responses compared to the SEE effects that are potentially catastrophic. One of the many advantages of non-catastrophic events is that we don’t need extreme accuracy in estimating event rates, provided that the more complex ways in which a device can respond to SEE – particularly SEFI events – has been properly identified. Catastrophic SEE effects, which require a great deal more care, will be discussed in Section V, following the discussion of SEE environments.

# III. Detectors

## *A. Basic Considerations*

There are many different types of detectors, but this section will be limited to optical detectors that are used from the UV to the mid-infrared range (~ 0.4 to 5 μm) and rely on the photovoltaic effect, along with a very limited discussion of detectors for longer wavelengths. In most cases the wavelength range of a specific detector technology is determined by the bandgap of the material, which establishes the upper wavelength limit. The lower wavelength limit is determined by the absorption coefficient, which increases very abruptly for materials with direct bandgap, but more slowly for an indirect material such as silicon. Fig. 8.compares the responsivity of silicon and InGaAs. HgCdTe detectors, which are not included in the figure, are sensitive at much longer wavelengths, up to 5 μm.

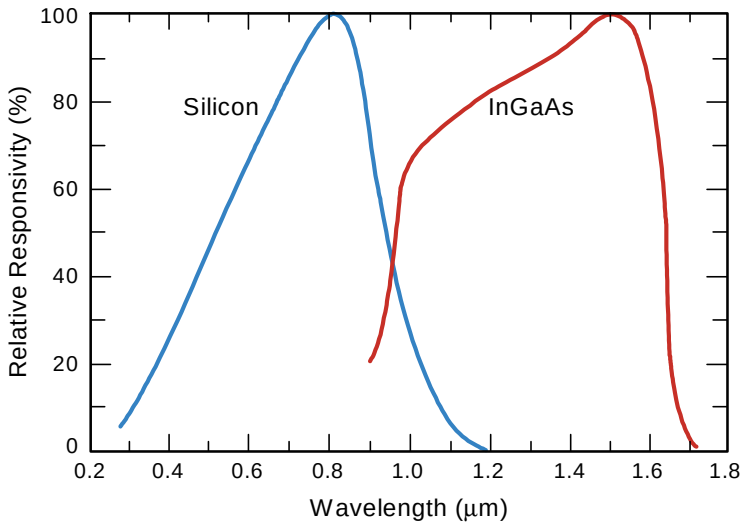


Fig. 7. Typical values of responsivity vs. wavelength for silicon and InGaAs detectors.

The basic types of detectors are listed below.

- P-N photodiode
- P-I-N photodiode
- Avalanche photodiode
- Charge-coupled device (CCD array)
- Active pixel sensors
- Infrared detector arrays

The key technical challenges are somewhat different for the various types of detectors. Noise is a critical concern for detectors that are intended to sense very low signal levels. Table 5 shows the approximate range of signal sensitivities for several different detectors, along with an "LET Limit" that is based on a first-order comparison of the charge sensitivity to the charge produced by an energetic particle in space. HgCdTe detectors are often required to sense extremely low signal levels, and are usually used at low temperature in order to reduce noise.

Table 5. Basic Properties of Optical Detectors

| Detector Type | Nominal Wavelength | Sensitivity (pC) | LET Limit for a Path Length of 1 μm |
|---|---|---|---|
| Photodiode | 0.8 μm | $10^{-2}$ to 1 | 1 – 100 MeV-cm$^2$/mg |
| Avalanche photodiode | 0.8 μm | ~$10^{-3}$ | 0.1 MeV-cm$^2$/mg |
| CCD | 0.8 μm | $10^{-4}$ | 0.01 MeV-cm$^2$/mg |
| HgCdTe array (77 K) | 2.5 μm | $10^{-5}$ | 0.001 MeV-cm$^2$/mg |

The sensitivity of these detectors varies by about 5 orders of magnitude. Those that are sensitive to very low LETs will experience large numbers of upsets during normal operation, which have to be taken into account when they are used in a specific application. Nearly all detectors are sensitive to upsets from protons (an indirect process) as well as heavy ions. When dealing with detectors, the effects of protons and reaction products from shielding have to be taken into account. as well as interactions from the primary particles.

For low-noise applications detectivity (D*) is used as a figure of merit. Fig. 8 compare D* for three different detectors with the theoretical limit for D* at 300 K. D* decreases rapidly at longer wavelengths, partly because the photon energy is inversely proportional to wavelength. HgCdTe are often used near the ideal limit, making them extremely sensitive to SEE.

A number of methods can be used to improve the performance of detectors in low level applications. Most noise terms are proportional to the square root of bandwidth, which allows the noise to be reduced by integrating the signal. Thus there is a tradeoff between integration time and noise.

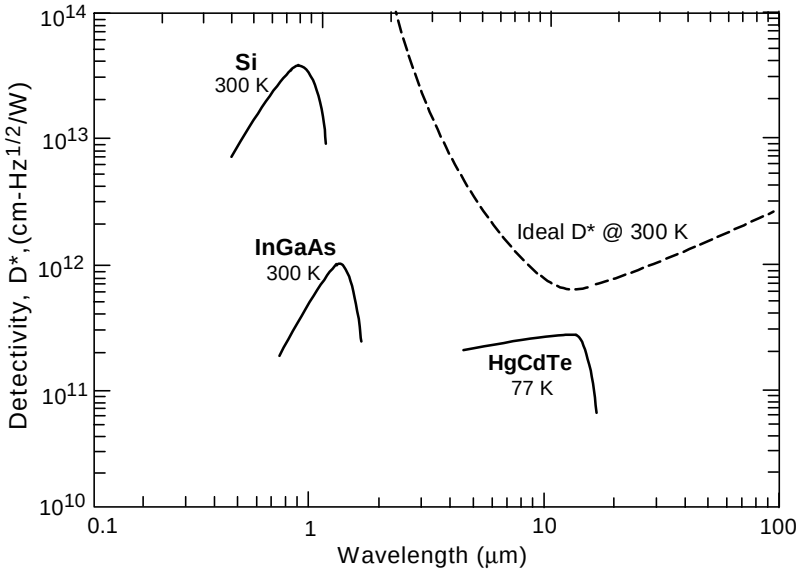


Fig. 8. Detectivity of various optical detectors. Particles with low D* are extremely sensitive to transient effects from particles in space, as well as reaction products from adjacent shielding.

We have to be particularly concerned about large-duration transients that can cause the detector (and its associated electronics to saturate), as well as transients of short duration that may introduce a higher overall noise level that can limit the ability of the detector to deal with low-level signals. A number of sophisticated approaches have been developed to reduce the sensitivity of detectors to radiation-induced transients, but a detailed discussion is beyond the scope of this guideline.

*B. Elementary Detectors Using Reverse-Biased Junctions*

P-n and p-i-n Detectors

Although it is impossible to eliminate the effects of heavy ions on p-n and p-i-n detectors, device geometry plays an important role. Fig. 9 shows a p-n photodiode where light is collected at a depth just beyond the depletion region, but charge is collected from an ion strike at distances well beyond the depth required for the optical response. These “dead” regions need to be minimized in order to reduce the amount of charge produced by heavy ions when they strike the device. One way to do this is to select detectors where the depth is tailored for a specific wavelength. Note that in addition to the region beneath the layer for optical absorption, charge from a heavy ion strike will also be collected from regions under the guard ring that do not contribute to light collection.

Ion strikes at large incident angles will produce far more charge than ions that strike the device at near normal incidence. This makes it undesirable to use large-area photodiodes (which is sometimes done to make alignment with optical sources less critical) because it increases the relative size of the spurious charge from an ion strike.

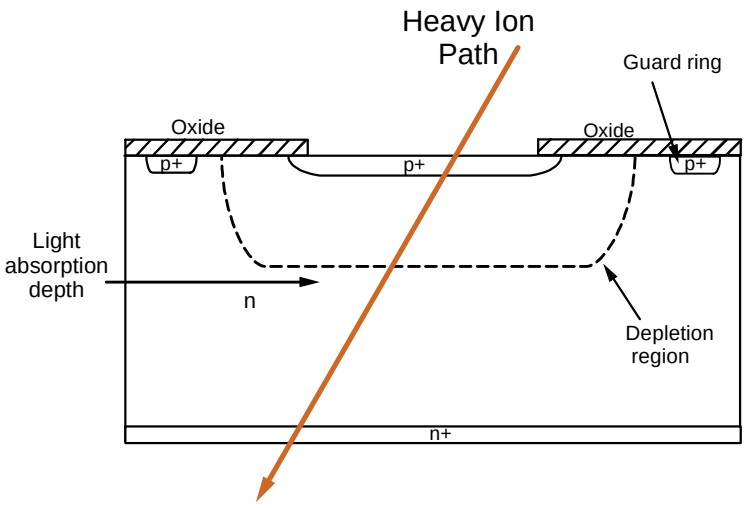


Fig. 9. Diagram of the path of a heavy ion strike in a p-n photodiode illustrating charge generation in regions that do not contribute to optical responsivity.

Because the absorption depth of silicon increases rapidly with wavelength, a detector optimized for performance at longer wavelengths will necessarily have larger signals from heavy ions compared to optimized detectors at shorter wavelengths. One way to deal with this is to use III-V detectors with direct bandgap at wavelengths in the near infrared instead of silicon detectors.

Avalanche Photodiodes

Similar issues occur for avalanche photodiodes. The avalanche process that increases photon sensitivity also affects charge from heavy ions or protons. This will affect the signal to noise ratio of an APD in radiation environments. Using direct bandgap semiconductors will reduce this effect, just as for conventional detectors, provided the APD structure is designed to minimize dead regions that can potentially contribute to charge collection from heavy ion strikes.

CCDs , APS and Other Array Detectors

The same principles apply to these detectors. However, it is possible to use long integration times and other system-related solutions such as elimination of large-amplitude noise spikes through signal processing.

Fig .10 shows a real-world example of the cumulative counts on a CCD from the SNAP satellite. The presence of large numbers of low-amplitude events has a large effect on low-level signals, but the event rate is much lower for higher amplitudes.

The application of HgCdTe detectors is far more complex. Those devices are typically used at low temperature to reduce noise, and are integrally connected to a CMOS readout chip that also operates at low temperature.

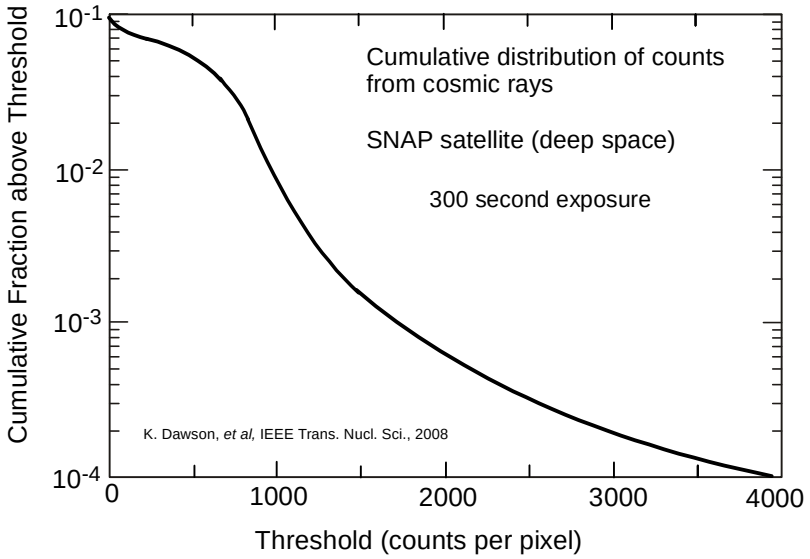


Fig. 10. Cumulative number of events during a 300-second integration time from a CCD in space.

## *C. Examples*

High-Speed Optocoupler

A simple example of SEE effects on optoelectronics is provided by a high-speed optocoupler. The device uses a high-gain, high-speed amplifier to boost the small signal from an internal photodiode (Fig. 11). For normal operation, a pulse from an internal light-emitting diode produces photocurrent in the photodiode that causes the output of the optocoupler to change state.

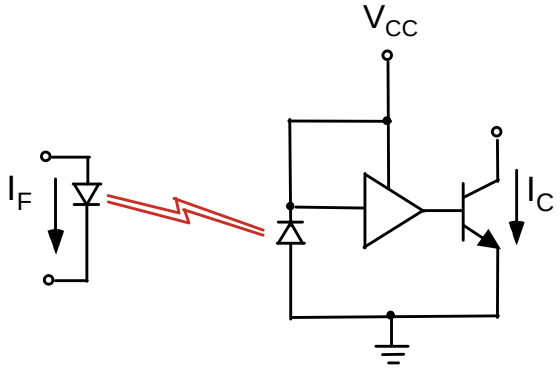


Fig. 11. Diagram of a high-speed optocoupler.

This device turns out to be extremely sensitive to SEE effects for two reasons: first, the high-speed amplifier allows the circuit to respond quickly to small signals; and second, the geometry of the internal photodiode is large (the diameter is ~ 500 μm) to allow easy alignment with the internal LED, which is on a separate assembly within the package. The large area of the photodiode results in a very long charge collection depth. The LET threshold for upsets in this optocoupler is about 0.3 MeV-cm$^2$/mg, an extremely low value. It is also unusually sensitive to upsets from protons due to the low threshold LET.

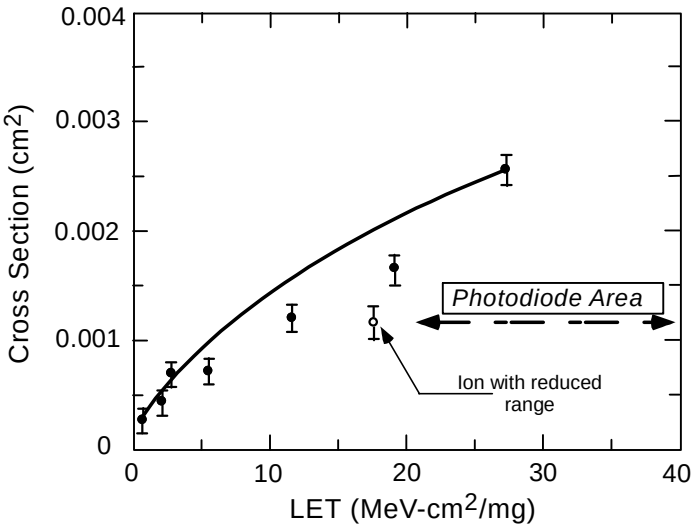


Fig. 12. Cross section vs. LET for the 6N134 high-speed optocoupler. The very low threshold LET is due to the sensitivity of the internal amplifier (~ 70 fC). The cross section increases above the area of the photodiode at higher LETs because the amplifier is also affected by heavy ions.

The event rate is very high for this device because of the low critical charge, approximately 70 fC, in combination with the relatively large area of the photodiode.

This simple optocoupler illustrates the basic issue for sensitive optical detectors: the area of the detector is typically very large compared to that of conventional integrated circuit structures, and it is connected to a high-gain amplifier. Those factors cause most optical detectors to be highly sensitive to SEU. The impact of the high SEU rate depends on the application. If the result of an error is a basic circuit response, then the impact can be very high.

Fiber Optic Receiver

A more complex example is that of a fiber optic receiver, where the receiver can tolerate a small number of errors. The number of errors that occur is affected by the optical power level. A common criterion for a receiver is that the bit-error rate (BER) is less than $10^{-9}$. The results in Fig. 13 show how the upset rate of a fiber-optic system is affected by the signal amplitude. The dashed curve shows the strong dependence of the bit-error rate on signal amplitude in an isolated laboratory environment when no radiation is present. The solid curve shows how the bit error increases when the receiver is exposed to 50-MeV protons.

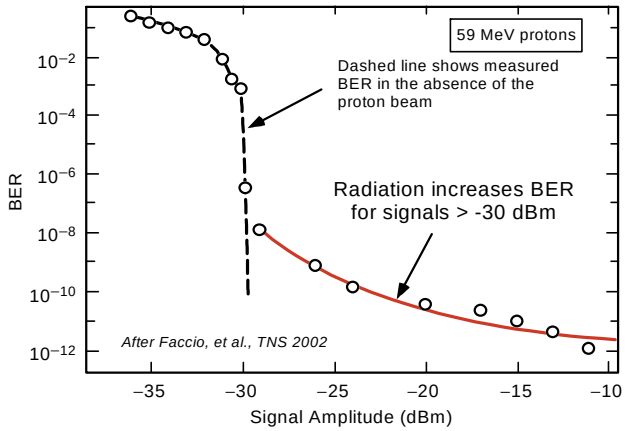


Fig. 13. Dependence of bit-error rate on the strength of the internal optical signals in an optical receiver during irradiation with 50-MeV protons.

In order to evaluate the performance of the receiver we have to take degradation of the internal components into account due to radiation and normal aging effects as well as the actual operating conditions of the receiver. It may be possible to use the receiver even with components that are heavily degraded during the mission. Note however that the very sharp increase in BER when the internal signal amplitude falls below -30 dBm introduces a very sharp "floor" for performance. We have to ensure that the receiver components will always allow it to operate above that threshold region.

We have some flexibility in choosing detectors for these applications. Fig. 14 compares the transient current that is induced in two different high-speed detector technologies by a heavy ion in space. The GaAs detector produces a higher current at very short times, but it dies out very quickly. The response of the silicon detector extends to much longer time intervals, and may cause larger errors, depending on the bandwidth of the system that used the detector.

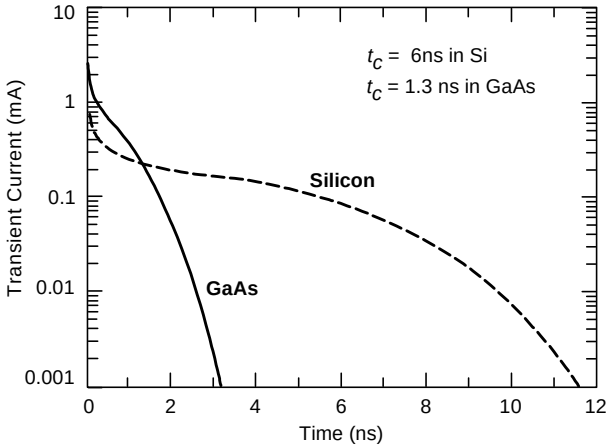


Fig. 14. Comparison of high-speed transient currents from silicon and GaAs detectors.

# IV. SEU Environments

## *A. Galactic Cosmic Rays*

Galactic cosmic rays occur everywhere in space, and they are the most important contribution to SEE effects for most electronic devices. There is a wide distribution of galactic cosmic ray particles in deep space, with LET values up to about 500 MeV-cm$^2$/mg. Fig. 15 shows the average daily flux, corresponding to solar minimum conditions, during which the GCR flux is highest. Note that the flux varies by about ten orders of magnitude as we go from particles with very low LET to those with LET values > 100 MeV-cm$^2$/mg. Except for a few devices that are extremely sensitive to SEE effects (such as the optocoupler discussed earlier), the main concern is for particles that have LET > 1 MeV-cm$^2$/mg. Note the very large decrease in the number of particles with LET > 30 MeV-cm$^2$/mg. The total number of particles with LET above that value is about 1 per year per cm$^2$, so if we can select devices that are unaffected by LET values below that threshold very few SEE effects will occur in typical spacecraft. Of course we have to take the "cosine law" into account, which increases the effective LET of that threshold condition from 30 MeV-cm$^2$/mg to about 75 MeV-cm$^2$/mg for particles that strike devices at more extreme angles.

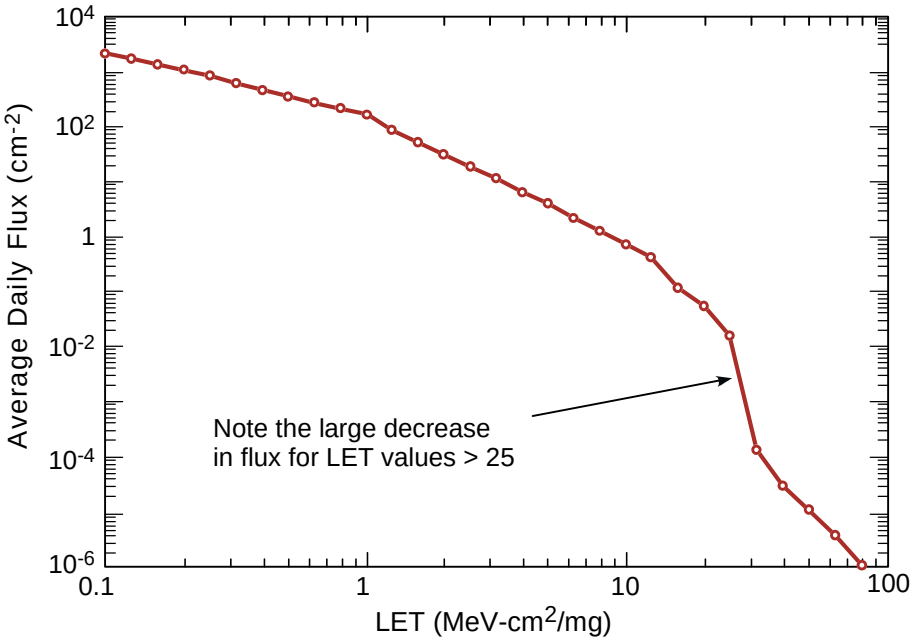


Fig. 15. Abundance of galactic cosmic rays during solar minimum conditions.

The sun's activity affects the distribution of GCR particles, reducing the average daily flux by about a factor of four during solar *maximum* conditions, when the sunspot activity is high, and there are large number of solar flares. Charged particles from the flares affect particles with lower energy in the GCR spectrum, which is the reason for solar modulation.

Shielding has relatively little effect on the GCR flux. Thick shielding can actually produce a slight increase in the number of particles with LET > 20 MeV-cm$^2$/mg because the particle LET actually goes up as the energy of highly energetic particles is reduced by the shielding. In practice, the amount of shielding that can be used in typical spacecraft has little effect on the GCR environment.

## *B. Solar Flares*

Basic Characteristics

We also have to be concerned about solar flares. Solar flare activity is correlated with sunspot activity, and we will use sunspot activity as an approximate measure of the condition of the sun. During an 11-year solar cycle, there are about four quiet years, followed by seven active years. Although solar flares can occur at any time, all of the intense flares have occurred during the seven-year active period of the solar cycle. (Solar modulation of the galactic cosmic ray intensity also corresponds to these quiet and active periods, remembering that the GCR abundance is depressed when the sun is active).

The intensity of solar flares decreases with distance from the sun, which will reduce the maximum solar flare intensity when Europa is near Jupiter. However, during transit – which will likely include gravitational assists that will keep it in the vicinity of the inner planets for several years – the solar flare intensity will be similar to that near the earth.

Solar flares have lower energies than galactic cosmic rays, and are more affected by shielding. The intensity of solar flares varies over a wide range. Even though most flares will have lower intensity, it is common practice to design electronic systems so they can withstand an extreme flare. Such flares persist for a period of about 24 hours, increasing the intensity of heavy ions by about four orders of magnitude. Fig. 16 compares the daily particle flux from GCR with such an intense flare.

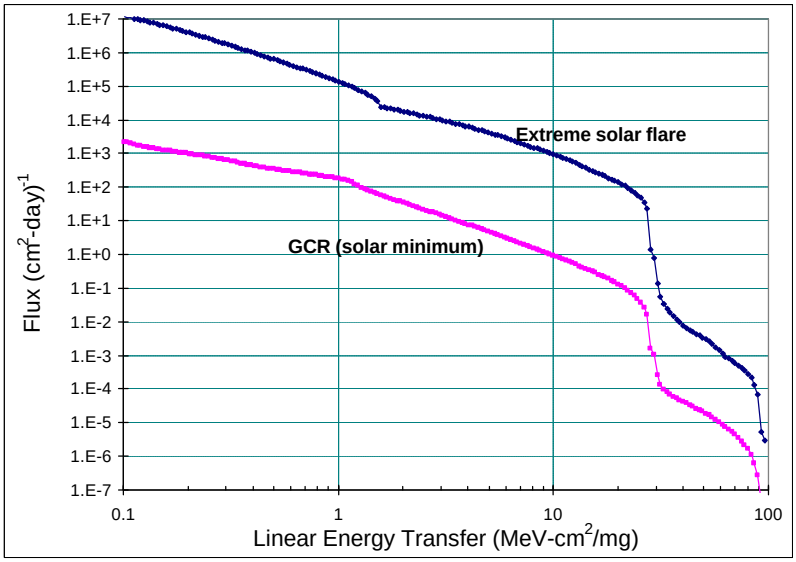


Fig. 16. Solar flare LET spectrum compared to the GCR spectrum for an extreme solar flare. Such flares persist for approximately 24 hours.

## *C. High-Energy Protons*

Energetic protons can also produce SEE effects. The "direct" LET of a proton due to its ionization wake is $\leq 0.025$ MeV-cm$^2$/mg, which is so low that it is usually impossible to cause an SEE event (there are rare exceptions to this rule, particular for detectors). In nearly all cases proton SEE effects are caused by secondary particles, that are the result of collisions (nuclear

interactions) with the material within a device. Fig. 17 compares direct ionization, the process for upset from GCR particles, with the indirect mechanism from proton nuclear reactions.

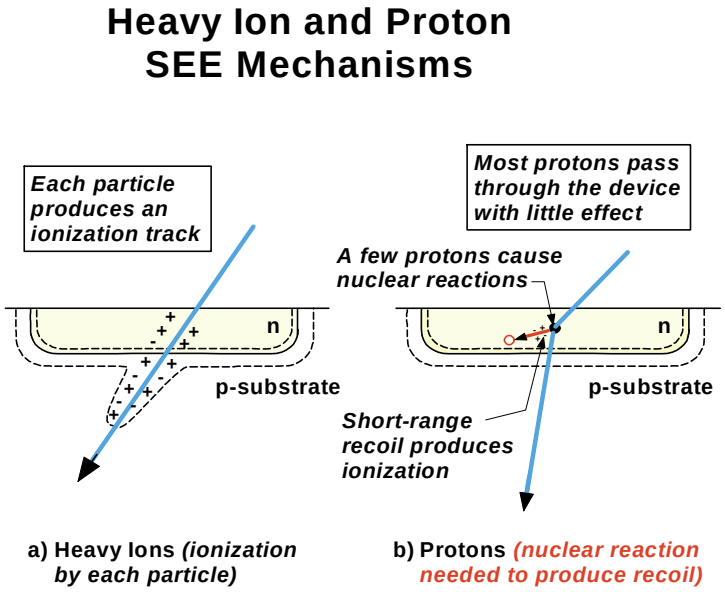


Fig. 17. Comparison of the direct ionization process for a heavy particle with the indirect process for protons, where a nuclear reaction produces a particle with higher atomic number (and higher LET) that produces the SEE effect in the device.

The range of the secondary particles from proton reactions is on the order of a few microns. Their effective LET – compared to that of a long-range particle – depends on the charge collection depth within a specific device. For a device with a very shallow charge collection depth the effective LET of the reaction particle – integrated over the charge collection region – may be about the same as for particles with long range. In silicon, the maximum LET from a 200 MeV proton is about 14 MeV-cm$^2$/mg. Thus, upset from protons cannot occur if the LET threshold for long-range ions is > 15 MeV-cm$^2$/mg.

For a device with a deep charge collection depth the recoil ion from a proton reaction can only travel a few microns. This reduces the effective LET (compared to long-range ions) to about 3-5 MeV-cm$^2$/mg.

Proton Spectra

The energy spectrum of protons in the earth's Van Allen belts depends on altitude and inclination. Fig. 18 shows proton spectra for two high-inclination orbits: a 705-km orbit, used in many earth observation spacecraft; and a higher altitude orbit, 1334 km, used by Topex-Poseidon and Jason. Two shielding conditions are shown. For both orbits the energy spectrum extends to about 500 MeV, with a peak energy between 20 and 50 MeV, depending on shielding.

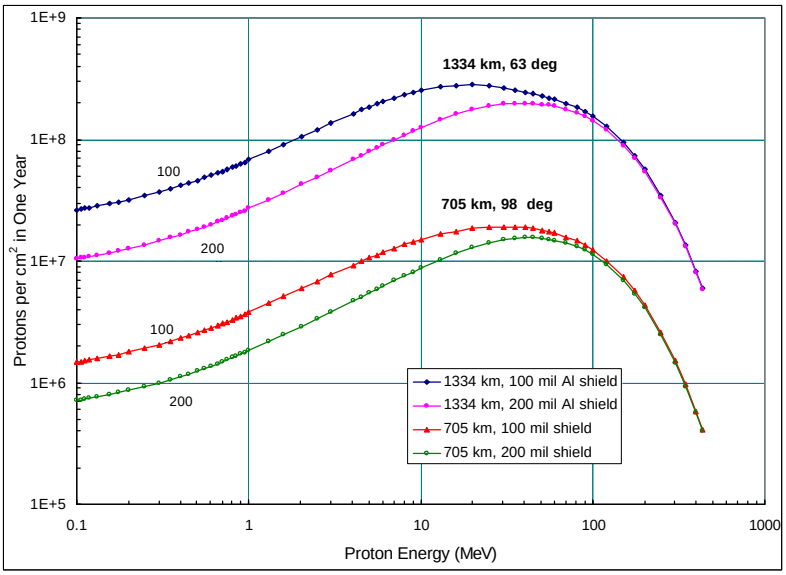


Fig. 18. Proton spectra for two high-inclination altitudes used by earth-orbiting satellites.

The proton energy spectrum of the Europa Explorer is different, falling off more rapidly at high energy. This is illustrated in Fig. 19 (the vertical axis is the integrated number of particles for the entire mission, not the annual number shown for the earth-orbiting spacecraft in the previous figure). Because there are fewer protons with high energy, proton upset will be less important for the Europa Explorer mission compared to typical earth-orbiting missions, and we will probably be able to ignore proton upset except for devices that have very low threshold LET values.. Nevertheless, we still have to consider proton upset effects for this mission.

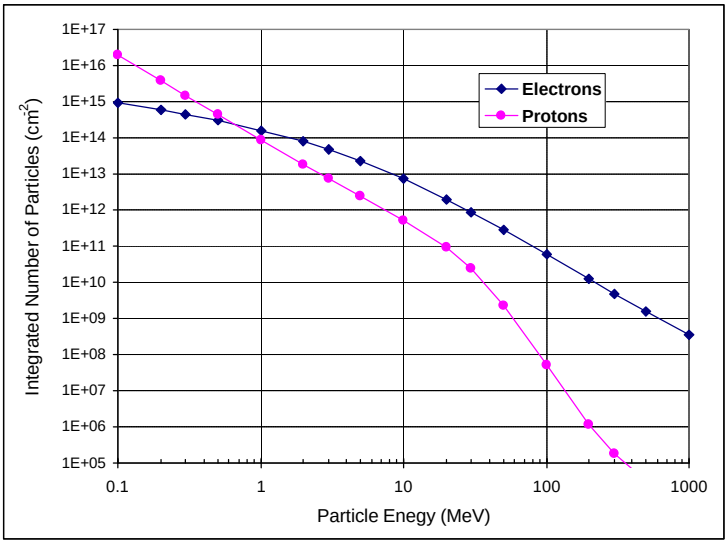


Fig. 19. Proton and electron spectra for Europa Explorer, integrated over the entire mission length. Due to the softer spectral shape, shielding will eliminate most of the protons that have sufficient energy to produce SEU effects, reducing the importance of proton upset for conventional electronics. However, proton effects will still be an important consideration for detectors.

# V. Catastrophic SEE Effects

SEE effects that are catastrophic, or potentially catastrophic, are of considerably more concern for spacecraft. We require better information about such effects compared to non-catastrophic events because it is usually not possible to correct them, other than through redundant circuit design. We also have to be concerned about the effect of processing changes, or even normal variations within a specific process, which can cause the conclusions about catastrophic effects to be different for different wafer runs of a specific circuit type. Radiation testing methods can also affect conclusions about these effects, and we must be scrupulously careful when we evaluate radiation test data to determine whether catastrophic effects take place as well as in calculating the expected probability that they will occur in the actual environment and circuit operating conditions.

## *A. Stuck Bits*

The first category of catastrophic effects is that of stuck bits. Stuck bits were not observed in older devices, but they do occur for modern devices with small feature size. The mechanism that is usually considered for stuck bits is *microdose* damage from the very intense ionization track of a high LET particle. It is a problem for parts with small feature size because the diameter of the ionization wake is on the same order, or even larger, than the gate area, producing a very high total dose in the localized region of the ion strike.

Fig. 20 compares the cross section for normal SEU errors to that of hard errors for a 64-Mb SDRAM. In this example the hard error cross section is about four orders of magnitude below the soft error cross section. In order to detect the hard errors it is necessary to use a sufficiently high fluence during testing so that the hard errors can be detected (they have a much lower overall cross section than the "normal" SEUs). It is also necessary to include ways to identify hard errors during the test. The number of hard errors increases with the LET of the incident particle.

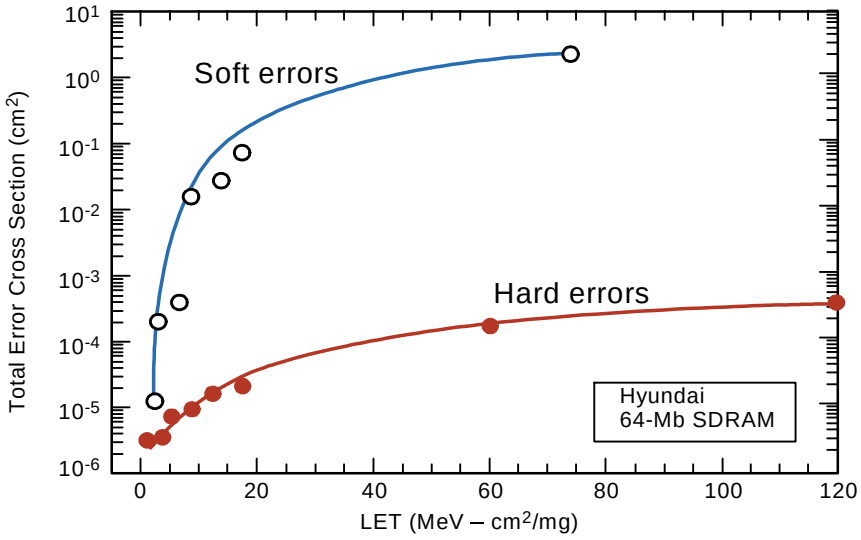


Fig. 20. Comparison of the cross section for soft errors with that of hard errors for a 64-Mb SDRAM.

The sensitivity of devices to hard errors continues to increase as semiconductor devices are scaled to smaller feature size. It is much easier to detect hard errors during tests of parts with large storage arrays. Stuck bits can be corrected for memories as long as the total number of stuck bits is not too high. It is far more difficult to correct for stuck bits in processors or controllers, which is an important consideration when aggressively scaled parts are considered for space applications because the total number of bits is so much smaller.

*B. Latchup*

Basic Characteristics

Latchup occurs when a p-n-p-n path is present within a circuit that can act as a four-layer switch, similar to a silicon-controlled rectifier. An example of such a path is shown for a CMOS process in Fig. 21. The p-n-p-n path is caused by parasitic bipolar transistors that are present because of the junction-isolation method used in most CMOS devices. No CMOS structures are involved. [Silicon-on-insulator (SOI) CMOS are an exception. SOI devices do not have these parasitic structures, and are immune to latchup, but nearly all CMOS devices with conventional isolation methods have the parasitic structure shown in Fig. 21].

A heavy ion in space can trigger latchup if the charge from the ion is high enough to exceed the minimum conditions for initiating latchup. Protons can also trigger latchup for circuits where the latchup threshold is below 14 MeV-cm$^2$/mg. Latchup is a concern for semiconductor manufacturers because CMOS structures can be triggered into latchup under normal operating conditions by electrical transients or out-of-synchronization voltage conditions. Except for hardened devices, manufacturers only consider latchup from voltages at the inputs, outputs, and power supply connections during operation, not from current pulses that occur *internally* when a device operates in space. The process and geometry changes that are periodically introduced by commercial manufacturers only consider electrically induced latchup. Consequently radiation tests need to be done on the specific devices used on the system. Using older data on latchup is unacceptable for a flagship mission such as Europa.

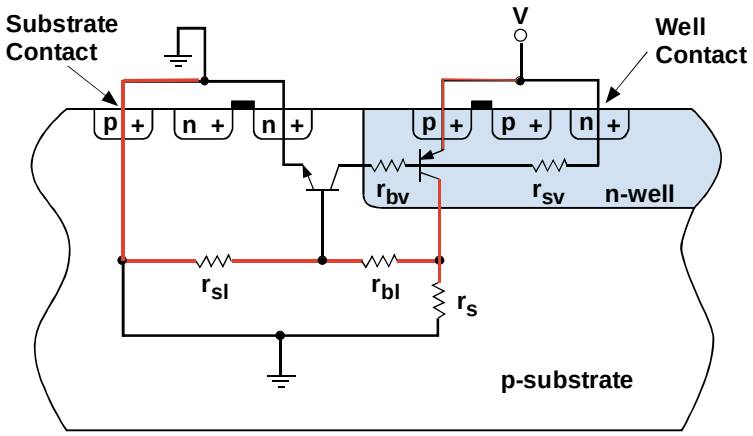


Fig. 21. Diagram of the p-n-p-n path in a CMOS structure.

Latchup is very sensitive to temperature, as shown in Fig. 22. The threshold LET decreases by almost a factor of two at high temperature, and the cross section increases as well. Consequently it is essential that devices are tested at the highest temperature expected in the application. Strip heaters can be placed underneath devices during testing to raise the

temperature. Tests that are done only at room temperature cannot be used to verify latchup compliance, although they can be effective in identifying devices with unacceptable performance.

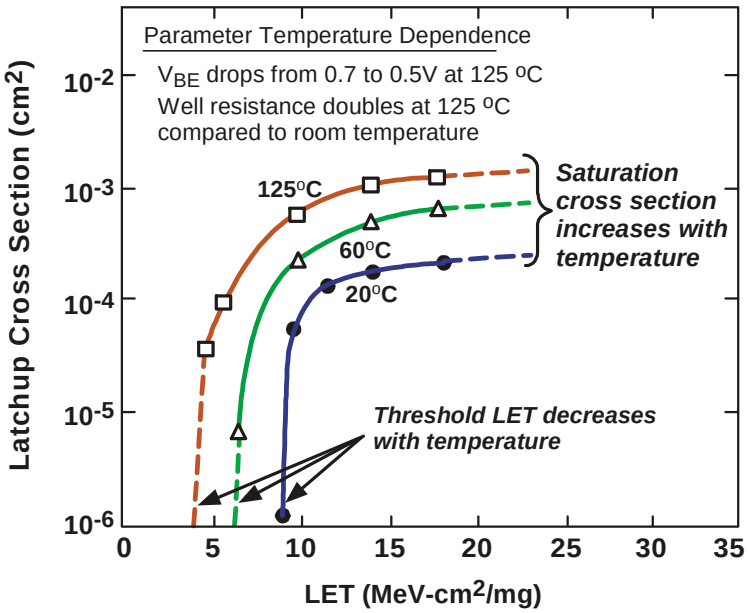


Fig. 22. The effect of temperature on latchup characteristic of a CMOS circuit.

When latchup takes place a large current occurs in the highly localized region of the latchup path. One of the effects that can take place is localized melting of the aluminum interconnects, as show in Fig. 23 (aluminum melts at a much lower temperature than silicon). In this example pressure from the melted aluminum has caused some of the material to be ejected from a silicon nitride layer that encases the metallization, producing a break in the metal line. In some cases the metal line still conducts afterwards, but the void in the metallization reduces circuit reliability.


Fig. 23. Melted aluminum ejected from a narrow metal trace during latchup.

Another example of catastrophic latchup is shown in Fig. 24. This is a simple circuit, without the multiple levels of metallization of the circuit in the previous example. The failure mode of this device is melting of the silicon region, which is evident from the dark globules that appear on the surface after it was tested. The melting temperature of silicon is 1415 ºC, demonstrating how high the internal temperatures can be when latchup takes place.

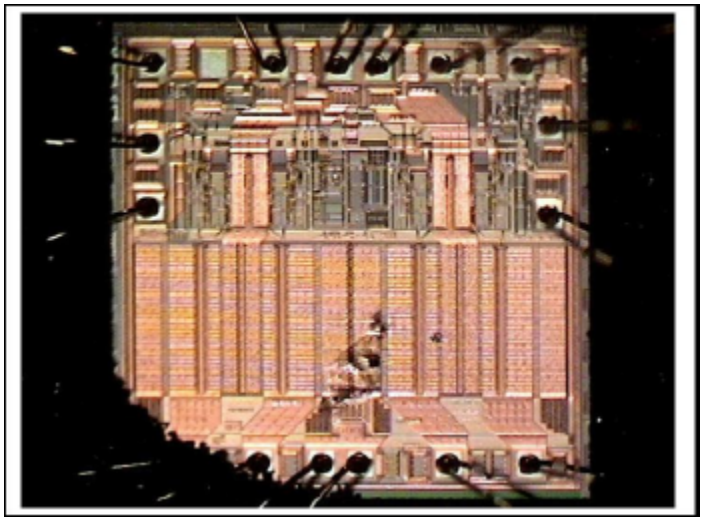

Fig. 24. Catastrophic damage in a circuit where the internal temperature is high enough to melt the underlying silicon.

Latchup Circumvention

When latchup takes place there is usually a sudden increase in the power supply current. It is possible to use that signature as a means of detecting latchup, with the idea of shutting off power to the circuit before catastrophic damage can occur. Although this approach is useful in selected cases, it is strongly discouraged for a long-duration high value mission such as the Europa Explorer. It is very difficult to show that latchup circumvention will work satisfactorily. There are several reasons for this, including the difficulty of making sure that all of the latchup events will actually be detected. Most circuits contain many different potential latchup paths, with different LET thresholds and cross sections as well as different current signatures. Even if the circumvention is successful small voids can occur within the metal from the high current during latchup (Fig. 23), decreasing reliability. Thus, latchup circumvention should only be considered as a last result.

Recommendations for Latchup

Most CMOS devices are sensitive to latchup. For a flagship mission such as Europa we have to take the potential impact on reliability into account even if a latchup event does not cause immediate destruction. The preferred approach is to avoid using devices that can be triggered into latchup by the space environment unless the parts are powered for only a small part of the mission length. If a device with a critical function is sensitive to latchup it may require very costly alternatives (such as substituting a custom ASIC, or building a circuit with the same functionality using parts that are not sensitive to latchup) in order to meet this requirement.

The first step is initial evaluations of latchup through testing. There are a number of cautions that must be observed for latchup testing and the evaluation of latchup test data. Many are

discussed in Section VI, but it is critically important to make sure that these tests are done correctly because of the potentially destructive nature of the effect. The key concerns are as follows:

- The electrical bias conditions must accurately reflect use conditions. The highly destructive latchup in the driver chip (Fig. 24) only occurred at voltages between 12 and 15 V.
- Due to the extreme sensitivity of latchup to temperature, elevated temperature conditions must be used for latchup evaluations.
- The total ion fluence used for testing must be limited in order to avoid damaging the parts in the course of testing and making an incorrect judgment about latchup susceptibility. This may require using a larger number of test samples and using fresh devices after the fluence has exceeded the point where it can affect the latchup-prone regions of a circuit.
- Ion range is extremely important. Unless a part uses an epitaxial substrate (which results in a shallow charge collection region) the range of the ions must exceed 50 μm.

### *C. Gate Rupture (SEGR)*

In power MOSFETs, a heavy ion can cause a permanent short in the gate region, increasing the leakage current and interfering with the ability of the gate voltage to control the device. A diagram of the mechanism that causes this effect is shown in Fig. 25. SEGR is affected by the drain-source voltage as well as the gate-source voltage because the intense ion track collapses the field beneath the gate, imposing part of the higher field in the underlying epitaxial region on the gate.

SEGR can take place with the drain voltage at zero (roughly corresponding to saturation), as well as conditions when the drain voltage is high. Devices need to be characterized at several different bias conditions. Those results can be used to generate safe operating curves. For general applicability it is necessary to develop curves that account for both the gate voltage and drain voltage effects. Often testing is done for a more limited set of conditions, particularly when the specific application conditions are known.

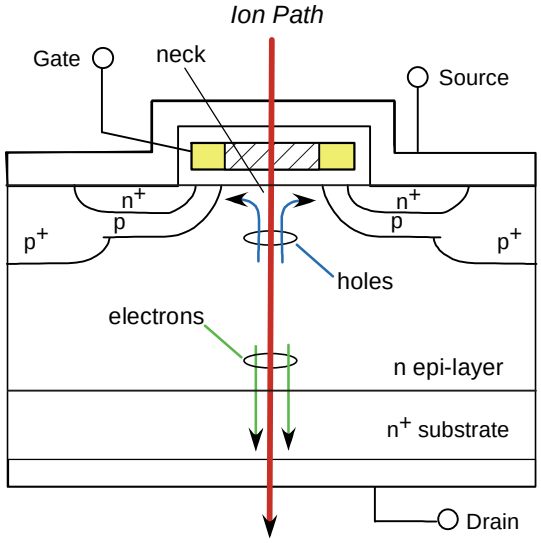

Fig. 25. Diagram of the flow of carriers within a power MOSFET when a heavy ion passes through the gate region.

Gate rupture tests are destructive. Furthermore, the results can vary somewhat for different samples, even if they are from the same lot. Several samples must be tested under each electrical condition and LET. A large sample size is required because the tests are destructive – each data point destroys a device! The usual test approach is to begin the test at a lower voltage (~ ½ the rated drain-source voltage), doing a series of tests with a particular ion where the drain voltage is stepped to a higher value for each subsequent test run until gate rupture (or burnout) occurs.

Fig. 26 shows an example of SEGR test data for a power MOSFET with a voltage rating of 115 V. The error bars show the range of experimental results for three units that were used (destroyed) at each LET. A total of 16 parts were required for this data. Only the drain-source voltage is shown, but the gate voltage used during testing was zero volts, corresponding to actual use conditions. Gate voltage also affects SEGR characteristics. If other gate voltage conditions were used, an additional set of 16 devices would be required to generate a similar set of data for the other gate voltage condition.

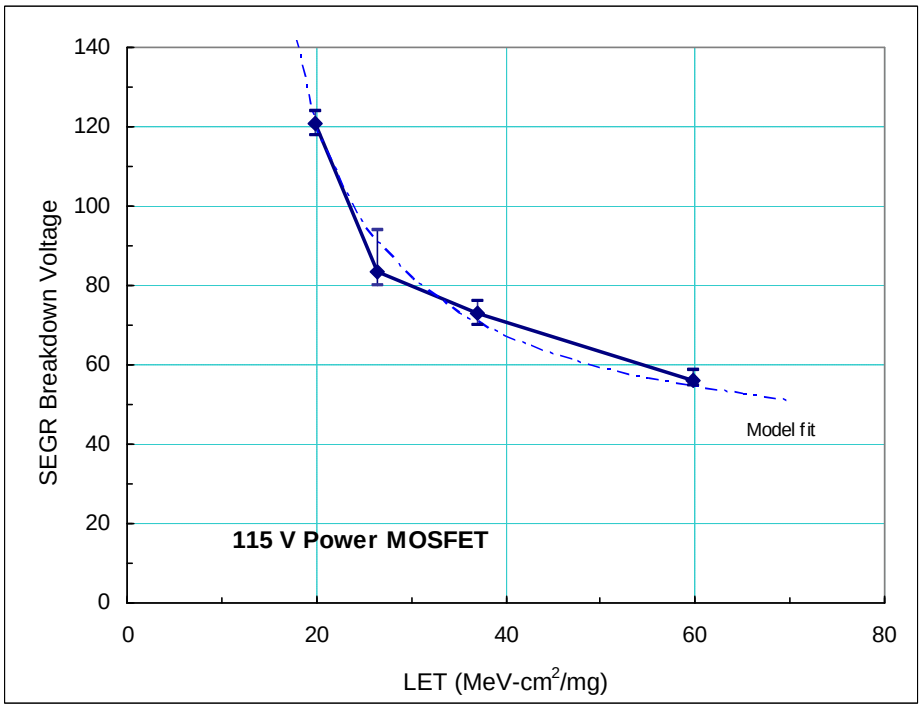


Fig. 26. Gate rupture test results for a power MOSFET with a drain-source voltage rating of 115 V.

SEGR data is used to establish derating guidelines for design, using an LET of 35 MeV-cm$^2$/mg for evaluation (SEGR effects do not increase with angle, which is the reason for using a lower LET value than for other SEE effects). In this case the part is rated by the manufacturer for a drain source voltage of 115 V, and the normal derating recommendation without considering SEGR would be to allow no more than 75% of the rated value to be used in the design.

When we take SEGR into account, the maximum allowable voltage for SEGR from the test results is 78 V. This value must then be derated by 75%, resulting in a maximum allowable voltage of 58.5 V for circuit applications.

*D. Single-Event Burnout (SEB)*

Single-event burnout can take place either in power MOSFETs or in power bipolar transistors. For power MOSFETs the only distinction between SEGR and SEB is the nature of the damage: SEGR causes a large increase in gate current, while SEB causes an increase in drain-source leakage along with the possibility of a short circuit (or partial short circuit) between the gate and source, or the gate and drain. The testing method is exactly the same. Often no distinction is made between the two mechanisms when test data are evaluated, resulting in just a single curve for the characteristics that cause either effect.

For bipolar transistors SEB tests are done by applying stepped values of collector-emitter voltage, and testing the device to a fixed fluence (usually $10^5$ ions/cm$^2$). The voltage is raised slightly, and the part is irradiated once again. That process continues until breakdown occurs.

The test results are similar to the SEGR example shown in Fig. 26. The same derating method is used to arrive at a safe collector-emitter voltage condition for design.

## VI. SEE Testing Concerns

### *A. Basic Issues*

With the exception of devices that are specifically hardened for such effects, devices fabricated with technologies that are sensitive to SEE nearly always require radiation testing as a means of determining (1) whether the effects occur, and how they affect the device; and (2) to determine the cross section and LET threshold with sufficient accuracy to allow a calculation of the expected probability (rate) in the environment. SEE testing is difficult and expensive. The parts have to be powered and actively evaluated during the time that they are exposed to the particle beam that is used to measure the device response. Travel and rental of accelerator facilities are involved.

Fig. 27 shows two engineers working on a complex board that is used to power the device during testing and interface between the device and the experimental area, which can be up to 50 feet away from the exposure area. In this instance the testing is more complicated because the device has to be placed within a vacuum chamber at the beam exit port with this particular facility.


Fig. 27. Example of a test chamber at a linear accelerator showing cabling that is required to test a complex device. The experiment is done in a vacuum chamber.

If the accelerator ions have sufficient energy and range it is possible to avoid using a vacuum chamber, a major advantage for complex parts. Fig. 28 shows a test board placed near the beam exit port that contains all of the peripheral circuitry needed to exercise the device during testing. The circuitry must be located close to the device that is in front of the beam line in order to do the tests at high speed. Note the cooling fan that is needed to keep the test devices and the peripheral circuitry from overheating during the test.

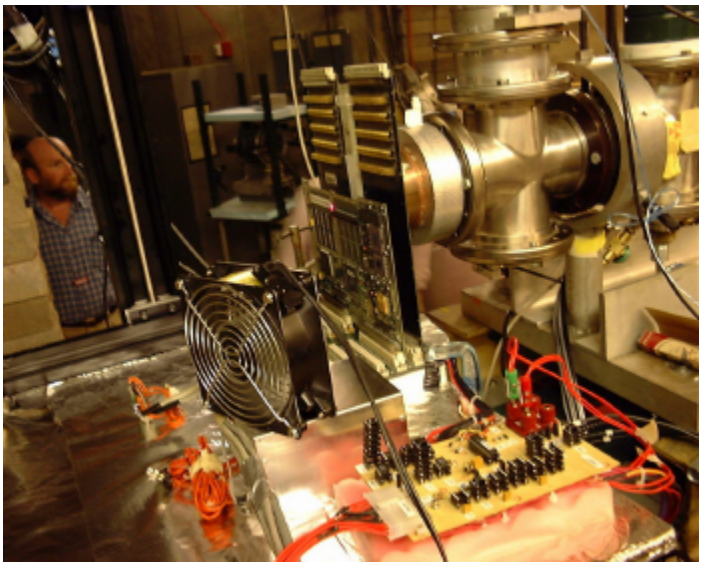

Fig. 28. Photograph of the test assembly used to test a complex gate array at a particle accelerator.

### *B. Packaging*

The range of the ions that are available at normal laboratory facilities is far lower than the range of the galactic rays in space. Usually the top of the package must be removed in order to allow the ions from the accelerator to reach the active region of the device. This has become an important practical problem as device technologies have advanced because of changes in package design. Fig. 29 shows a cross section of a modern device that uses "flip chip" bonding. The device is inverted, making contact to leads at the surface by means of special solder balls that are located on a ceramic substrate. These packages can accommodate very large numbers of leads, and may be the only package that can accommodate complex chips with > 300 leads.

Even if the chip could be removed from the package, often there is no "equivalent" package that would allow the part to work satisfactorily with conventional die attach from the back and lead bonding from the top surface. The only way to deal with this is to use ions with extremely long range that can penetrate the entire chip from the back, or to mechanically thin the die to reduce the thickness for compatibility with the more limited ion range provided in normal facilities. Thermal issues further complicate this problem. In some cases a heat sink is used on the top of the inverted die in a flip-chip package which must be removed for radiation testing.

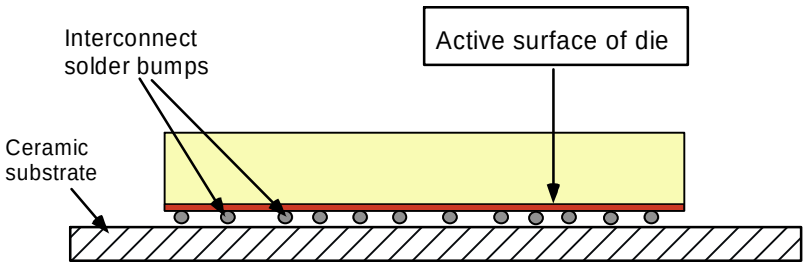


Fig. 29. Diagram of a flip-chip package. Ions must penetrate the entire die thickness in order to test such devices at radiation facilities. In most cases the device must be mechanically thinned because ions that are available at typical radiation facilities do not have enough range to penetrate the normal die thickness.

*C. Ion Range and Angle of Incidence*

The range of the particles used for testing is one of the most important considerations. For modern devices particle range must take the additional thickness of multiple levels of metallization into account as well as the charge collection depth within the active device. Brookhaven National Laboratory (BNL) has a particle accelerator that is frequently used for SEE testing. The range of the particles from that facility are limited, and can only be used to test devices with shallow charge collection depth. Fig. 30 shows how the LET of particles with high LET from that facility change as they travel through silicon. For Iodine, the value of LET at the surface is 60 MeV-cm$^2$/mg. It falls to half that value at about 27 µm, without considering that the effective distance may be reduced by surface layers up to about 10 µm. The highest LET particle from BNL is gold, with a surface LET of 8 3MeV-cm$^2$/mg. Its range is much lower than that of Iodine. Furthermore, if we attempt to increase the effective LET of Iodine by tilting the device to increase the effective LET the range is even lower. Thus, it is very difficult to use this facility to ensure compliance with the maximum LET testing requirement unless the device has a very shallow charge collection region.

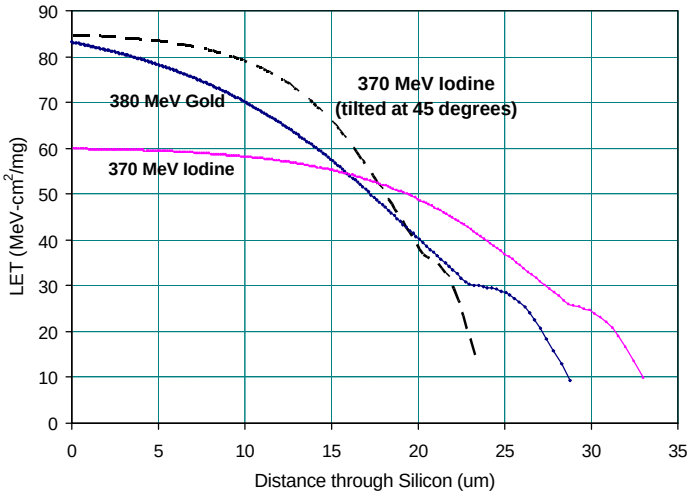


Fig. 30. LET vs. distance of travel in silicon for gold and iodine ions at the Brookhaven National Laboratory. The LET value is reasonably near that of the surface LET for approximately 10 µm, but falls rapidly as the distance increases. The particles have insufficient range for most devices. The short range is of particular concern for latchup. In some cases devices that have not exhibited latchup in tests at this facility have latched when tests were done at facilities with longer range (~ 100 µm)

It is common practice to tilt devices during SEE testing to increase the effective LET (see Fig. 1 and the related discussion). The validity of this assumption depends on several factors, including ion range. Data in Fig. 30 for the iodine beam at a 45 º incident angle shows nearly the same LET profile as gold at normal incidence. Furthermore, if we integrate the charge over a path length of 30 µm there is very little difference between the charge generated by iodine at normal incidence and the charge generated when the ion strikes the device at the 45 º angle. The range calculations used to generate this figure do not take dead layers at the surface from passivation coatings and metallization into account. For modern devices with several metallizatoin layers the “dead” region can be 5 µm or more, causing less charge to be generated when the beam strikes the device at large angles. Therefore we have to estimate the charge

collection depth of the device before using the increased LET provided by a strike at non-normal incidence in evaluating SEE data.

The other factor that is important in evaluating angular effects is the effective dimension of the charge collection region. For shallow structures, the cosine law assumption is usually valid. However, many devices collect much of the charge by diffusion instead of drift, resulting in a charge collection region that can be considered nearly spherical rather that a parallelopiped. For a spherical region the charge generated by a strike at angle is independent of angle, invalidating the cosine law assumption.

We do not necessarily have to know the details of the charge collection region. Test data often provides direct evidence of cases where the cosine law fails. Fig. 31 shows test results for a 512-Mb DRAM that was tested with several different incident angles (the x-axis is effective LET, which assumes that the cosine law applies). It is obvious from these results that the cosine law fails because of the large differences in results when we plot the data using effective LET.

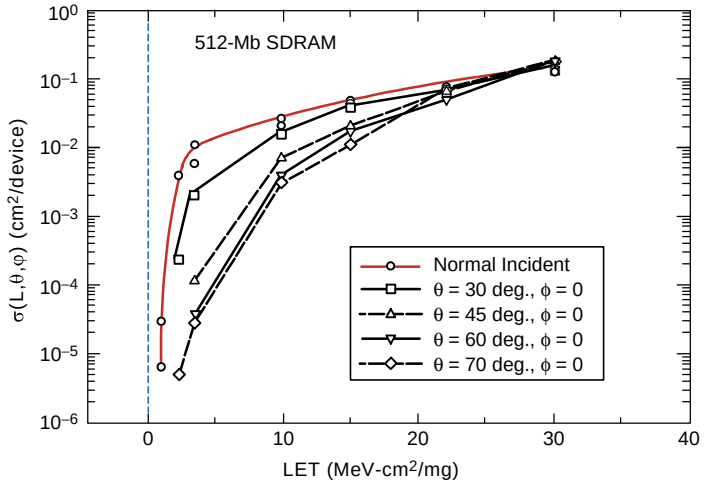


Fig. 31. Test results for a 512-Mb DRAM illustrating a case where the "cosine law" clearly does not apply. The x-axis is effective LET, which assumes the cosine law.

The validity of the cosine law is particularly important for catastrophic effects, such as latchup and SEGR. It often applies to latchup, provided there is sufficient ion range, but can never be applied to SEGR (or SEB).

### *D. Statistical Concerns*

SEE phenomena are statistical in nature because of the random way in which ions strike a device in space, and most accelerator facilities scatter the beam to provide a random pattern. Only limited conclusions can be made about test results where only a few events are observed because of these statistics. If > 20 events are observed, the statistical uncertainty is

$$\sim \frac{1}{\sqrt{N}} \qquad (2)$$

where N is the number of events.

A somewhat more complicated interpretation is required where only a few counts are observed. A common criterion used for radiation testing is that at least 100 events should be observed, producing an uncertainty of 10% in the cross section calculated from the experiment. This condition is often violated. It is important to realize that very large statistical error bars

result for a small number of events, which must be taken into account in the interpretation of experimental results.

The statistical limitations of data points where only a few events are observed are often ignored when SEE results are analyzed. This can lead to the wrong conclusion, and must be understood in order to use SEE data for an important mission such as Europa. Table 6 shows the upper and lower statistical limits for various numbers of events. The factors in the table should be applied to the *apparent cross section*, which is the cross section that is calculated from the actual number of events and the fluence. For example, if only 4 events are observed, the apparent cross section is (4)/(particle fluence). From the table, the lower limit is (1)/(particle fluence) and the upper limit is (10.2)/(particle fluence). Thus, even though four events were observed we have a statistical uncertainty of a factor of 4 for the lower limit, and 2.55 for the upper limit. The uncertainty is much higher when even fewer events are observed.

Table 6. Statistical Limits for 95% Confidence for Various Numbers of Observed Events

| N | 95% Limits | |
|---|---|---|
| | Lower | Upper |
| 0 | 0.0 | 3.7 |
| 1 | 0.1 | 5.6 |
| 2 | 0.2 | 7.2 |
| 3 | 0.6 | 8.8 |
| 4 | 1.0 | 10.2 |
| 5 | 1.6 | 11.7 |
| 6 | 2.2 | 13.1 |
| 7 | 2.8 | 14.4 |
| 8 | 3.4 | 15.8 |
| 9 | 4.0 | 17.1 |
| 10 | 4.7 | 18.4 |
| 11 | 5.4 | 19.7 |
| 12 | 6.2 | 30.8 |
| 13 | 6.9 | 22.3 |
| 14 | 7.7 | 23.5 |
| 15 | 8.4 | 24.8 |
| 20 | 12.2 | 30.8 |
| 25 | 16.2 | 36.8 |
| 30 | 20.2 | 42.8 |
| 35 | 24.3 | 48.7 |
| 40 | 28.6 | 54.5 |
| 45 | 32.8 | 60.2 |
| 50 | 37.0 | 65.9 |

Counting statistics are not the only factor that affects SEE data. We also have to consider the uncertainty in the particle LET, which may be higher or lower than the surface LET for the particle, depending on the particle energy. The number of devices that are used for testing is also important. Usually there are some differences in the cross section when we test more than one device, and those differences also have to be accounted for when SEE results are analyzed.

### *E. Device Damage*

For SEE tests, there is a tradeoff between the particle fluence and the gradual buildup of radiation damage within the device as increased numbers of heavy ions are used during the course of an SEE test. Heavy ions have far more charge within there nuclei compared to protons, which increases the amount of displacement damage that they produce. This can be a very important interference effects during device testing because the usual approach is to use the same devices for several different test runs with various types of ions. The total ion fluence can exceed $10^9$ /cm$^2$.

Table 7 shows the damage for various types of ions used in SEE testing, normalized to the damage produced by 50-MeV protons. The table assumes that the total fluence for a single test

run is $10^7$ /cm$^2$. The values show that the relative damage produced by the ions is between 1300 and 6200 times the damage produced by protons. The calculations are only done for the value of LET at the surface, and do not take account the even stronger increase in damage that occurs if the ions come to rest within the charge collection region of a device.

Table 7. Equivalent 50-MeV Proton Fluence from a Fluence of $10^7$ ions/cm$^2$ for Various Ions Used in SEE Testing.

| Ion Type | Energy (MeV) | Range to Bragg Peak(μm) | Z | Relative Proton Damage Fluence* | Surface LET (MeV-cm$^2$/mg) |
|---|---|---|---|---|---|
| Krypton | 1296 | 149 | 36 | 1.3 x $10^{10}$ | 25.4 |
| Silver | 1634 | 130 | 47 | 2.2 x $10^{10}$ | 38.5 |
| Xenon | 1934 | 125 | 54 | 3.0 x $10^{10}$ | 47.3 |
| Praesodymium | 2114 | 117 | 59 | 3.5 x $10^{10}$ | 53.8 |
| Tantalum | 2715 | 107 | 73 | 5.3 x $10^{10}$ | 79.2 |
| Gold | 2955 | 102 | 79 | 6.2 x $10^{10}$ | 80.2 |

*Damage from 1 x $10^7$ ions/cm$^2$, normalized to equivalent 50-MeV proton damage

If the cumulative 50-MeV proton fluence from SEE testing is ~ 5 x $10^{11}$ p/cm$^2$ or more, the minority carrier lifetime will begin to be affected, reducing the amount of charge that is collected from an ion strike. For long range ions that travel well beyond the charge collection region (assumed to be about 50 μm), this will occur when the total ion fluence is about $10^8$ ions/cm$^2$. Consequently it may be necessary to use fresh devices after a fluence of that magnitude is exceeded during a test run.

Although displacement damage can be important for all SEE phenomena, it is particularly important for latchup because the internal parasitic transistors that cause latchup to occur are directly affected by displacement damage. Latchup tests with high cumulative fluences on individual parts may be misleading, changing the threshold LET and cross section, or even eliminating latchup in some cases.

# VII. Qualifying Devices for SEE Effects

*A. General Considerations*

The interplay between device scaling, which has reduced the dimensions of the transistors used within integrated circuits; device complexity, which results in highly complex circuit functions that are difficult to evaluate; and new SEE phenomena, such as stuck bits, complex functional interrupt signatures, and multiple-bit upset has increased the difficulty of qualifying devices for SEE effects in the space environment. The net effect has been to move from the basic single-event upsets of earlier generation devices to a complex set of responses that are not only difficult to characterize, but are application dependent.

As a result, it has become far more difficult to develop a methodology for part qualification. In extreme cases, such as microprocessors, it may be impossible to qualify devices without using the specific software that is used in applications.

Although it is still possible to generate curves of cross section vs. LET, and then to calculate the number of events expected in a specific environment, the impact depends on the specific way in which the device is used within a circuit or subsystem. Designers must understand the full impact of SEE effects on the devices that are used in order to meet the overall requirements for spacecraft and instrument performance.

It is also important to recognize the difficulty of implementing and interpreting SEU tests. Most of the details were discussed in the previous section, but it is worth repeating that the test conditions must overlap actual use conditions, particularly for catastrophic SEU effects.

*B. Device Variability*

It is important to understand that SEE effects can be highly variable. This can occur because of normal processing variations, even if the basic design and processing rules do not change, as well as cases where deliberate changes are made to improve yield or performance by the manufacturer. Therefore it is essential that radiation testing is done on the specific lots that are used in flight hardware, particularly for catastrophic SEE effects such as latchup. This limits the usefulness of older test data. Although archival data may be very helpful in initial part selection, changes in the way that parts are manufactured can cause drastic changes in their response in the space environment. For example, catastrophic latchup in the driver chip, shown earlier in Fig. 24, did not occur in earlier production lots.

Device variability has still another impact. It is anticipated that Europa will provide design data for the majority of the parts that are used. However, some of the data that justifies inclusion of parts on the Approved Parts and Material list will be from older lots of devices, not the actual lots used for production. There will likely be cases where the response of parts in the flight lot are not the same as earlier lots. In the case of latchup, this could require substitution of alternative part types or restrictions on power supply voltage, depending on the specific differences that occur.

*C. Special Issues for Hardened Device Technologies*

Parts that are specifically hardened for SEE effects present a unique challenge. They are nearly always a better choice than unhardened parts, but we have to be particularly careful about the way in which they are used. One example is the RAD-6000 microprocessor, which has been

successfully used on many JPL systems. SEE test results from the manufacturer are shown in Fig. 32. Two points are important. First, the upset rate is low, but it is not low enough to prevent a small number of upsets occurring during an extended space mission. This means that we have to allow for some upsets that could potentially "scramble" the performance, which for this type of part could involve spacecraft control. Second, the test results are very different when the tests are done under static conditions compared to tests done in a high-speed dynamic mode that is more representative of application conditions. Despite the fact that it is hardened, the "tail" at low LETs extends below 10 MeV-cm$^2$/mg, a region where there are many more ions. The device is also susceptible to protons, even though the cross section is very small, which may be a concern during an intense solar flare.

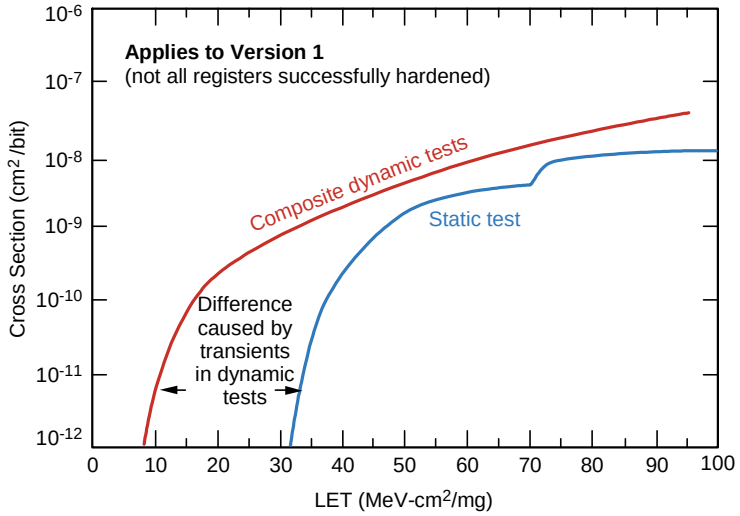


Fig. 32. SEU data for a hardened microprocessor showing a low LET "tail" that must be accommodated when the device is used in space. Although the upset rate is low, some upsets will take place despite the fact that the part is hardened against this environment.

Similar problems can occur in hardened memories, where the overall SEU response is far better than for unhardened devices, but "tails" in the SEU response curve or functional interrupt mechanisms mean that the application of the part is not fully transparent. Internal transients in memories or other digital circuits can also produce low probability upsets.

# VIII. General Recommendations and Requirements

*A. Overall Perspective*

As discussed in the Introduction, not all active components are affected by SEE. Most discrete bipolar transistors (with the exception of parts with breakdown voltage > 100 V, where SEB is a potential problem) and many simple logic devices are immune because they have relatively large device area and relatively slow response times.

For space applications we have to be concerned about the effects of particles with LET values up to 110 MeV-cm$^2$/mg for most SEE where the effective LET increases with the angle of incidence. It may be possible to relax the upper value to 75 MeV-cm$^2$/mg for selected cases where very few parts are used within the total system. Table 8 summarizes various SEE phenomena along with the basic device technologies that are sensitive to such effects. The shaded rows are for effects where the damage is catastrophic. The LET limit is lower for SEGR and SEB because those effects do not increase with the angle of incidence of the incoming particle.

Table 8. Summary of SEE Effects for Various Device Technologies

| **Effect** | **Angular Effect** | **Maximum LET (MeV-cm$^2$/mg)** | **Temperature Requirement** | **Device Technologies** |
|---|---|---|---|---|
| SEU | Yes | 110 | 25 ºC | All logic devices with internal storage elements, as well as mixed-signal parts |
| SET | Yes | 110 | 25 ºC | All linear devices<br>Voltage regulators<br>Voltage references |
| SEL | Yes | 110 | **125 ºC** | CMOS and BiCMOS (except SOI) |
| SEGR | No | 35 | 25 ºC | Power MOSFET |
| SEB | No | 35 | 25 ºC | Power MOSFET and power bipolar transistor |

The requirements are supported by studies and data in the literature, as well as field results from spacecraft. However, there are cases where it is not possible to fully meet them. One of the most difficult problems is that of dealing with special packages, where it is not possible to get direct access to the top of the die (see the discussion in Section VI).

We also have to be concerned about the total part count when SEU rates are interpreted. Individual devices are available now that contain orders of magnitude more storage elements compared to older devices. This introduces the possibility that the system will not be able to accommodate an upset rate that was formerly considered to be benign because the total number of devices – and aggregate number of stored bits - is so large.

*Single-Event Upset*

General Characterization Requirements

All microcircuits containing bistable storage elements (flip-flops, counters, registers, and memories) shall be tested over a range of LET values up to 90 MeV-cm$^2$/mg. Test data must be provided at a minimum of four LETs. For devices with more than 1000 storage elements the tests must be able to distinguish between single and multiple bit errors, as well as stuck bits. Test data must be reported for all three types of errors.

The range of the ions must be at least twice the charge collection depth, accounting for additional layers of metallization and interconnect on the surface. If the charge collection depth is unknown, then the range of the ions must exceed 50 µm.

The fluence used for testing must be > $10^7$ ions/cm$^2$. Because of concerns about radiation damage, test must be done on at least two parts at the highest test fluence that have *not* been exposed to ions with lower LET. The results for those two devices shall be compared with that of other devices in the test sample to determine whether damage from the high fluences required by the tests to reduce statistical counting errors have affected the results.

Except for hardened devices, SEU test results are required for each wafer lot unless existing test data is for devices that have the same mask set as the devices in wafer lots procured for use in the system.

Special Issues for Hardened Device Technologies

Existing test data can be used for hardened device technologies, provided that the data meets the general characterization requirements in the previous sub-section and that the manufacturer includes SEU upset rates in the device specifications.

In some cases data provided by manufacturers of hardened devices does not cover the higher LET range that is needed for a long-duration mission such as the Europa Orbiter. For example, a hardened microprocessor from an offshore manufacturer included an upset rate that was based on test data that did not extend to LET values > 40 MeV-cm$^2$/mg. When tests were done at higher LET values, the event rate was much higher because the circuit technique used for hardening was no longer effective. Acceptance of data from a manufacturer is conditional: the test conditions must meet the overall requirements for radiation testing.

Overall Requirements for SEU (including MBU and SEFI effects)

Although it is much easier to deal with devices that are immune to SEU effects, the final requirement is that the overall system design can tolerate upsets when they occur. The overall requirements are as follows:

1. No upsets observed during LET testing up to a maximum LET of 90 MeV-cm$^2$/mg, or
2. Verification of a device bit error rate < $10^{-10}$ errors per bit day from galactic cosmic rays. In addition, the total number of devices used in the system must be determined in order to verify that this error rate is low enough to make the system nearly immune to SEU effects.

A third requirement can also be invoked, which goes beyond the part requirements and requires a waiver. That requirement is "*verification that the application of the component within the circuit and subsystem can tolerate the SEU effects that are observed*." Verification of the third requirement is far more difficult. It can only be implemented if a thorough set of test characterization data are available, with a clear distinction between simple upsets and the more

complex effects of MBU and SEFI. The starting point is calculation of the expected upset rate from galactic cosmic rays and solar flares. Although it is complicated, this is the basic process that has been used in the past for solid-state recorders where the upset rate of the internal memory chips is high enough to produce more than 100 upsets (within the entire array) in a single day from galactic cosmic rays.

*Single-Event Transients*

In general radiation test data must be available for all digital and analog microcircuits. The test conditions must envelope actual system use conditions. A circuit and/or subsystem analysis must be done to demonstrate that SETs will still allow the circuit or subsystem to meet overall requirements. An alternative approach (in lieu of data) is to demonstrate that the circuit application can tolerate transients with an amplitude equal to the power supply voltage and a duration of 20 μs.

Transient pulses from analog and mixed signal devices may exceed the maximum safe operating conditions of other circuits that are connected to them, causing permanent damage. The circuit and subsystem analysis must take such effects into account.

Test requirements for SET are the same as for SEU, discussed in the previous sub-section. Damage from high fluences during testing can affect SET results, and the test data must demonstrate that such damage is not a factor in the results.

*Single-Event Latchup*

All CMOS and BiCMOS devices, including those with epitaxial substrates, shall be tested to determine whether they are affected by latchup when they are exposed to galactic cosmic rays. Latchup tests must be done at elevated temperature (usually 125 ºC). Tests should be done on samples from the flight lot because latchup characteristics can change, even with normal processing.

The basic requirement is that no latchup is observed up to an LET of 75 MeV-cm$^2$/mg. The ions used for testing must have an effective range of 50 μm after correcting for losses in circuit overlayers. The fluence used for testing should be > $10^7$ ions/cm$^2$ for each test run. Two devices that have not been irradiated in previous test runs shall be irradiated at the highest LET value, verifying that latchup did not occur on fresh devices.

The use of devices that exhibit latchup is strongly discouraged. However, it is possible to use devices that have threshold LET values between 35 and 75 MeV-cm$^2$/mg provided that the latchup probability is below $10^{-5}$ per year. The data used to determine the latchup probability must be approved by a radiation specialist. The total number of latchup-prone parts used in the system must be known in order to determine whether the net effect on system reliability from such latchup events is low enough to meet system requirements.

*Single-Event Gate Rupture*

All power MOSFETs shall be evaluated for single-event gate rupture. The test results must overlap the gate-source voltage and drain-source voltage in circuit applications. The tests should be done for an LET value ≥ 35 MeV-cm$^2$/mg, using ions that are at normal incidence. The fluence for each test run must be ≥ $10^6$ ions/cm$^2$.

If SEGR occurs, the device is destroyed. Consequently unusually large sample sizes are required. Test data for a minimum of five parts is required at each LET value and electrical condition where the tests are done.

Ion range is particularly important for SEGR. The minimum ion range depends on the voltage rating because of basic requirements on the device design, which cause the depth of the region beneath the gate to increase for devices with higher voltage ratings. The range requirements are listed in Table 9.

Table 9. Minimum Ion Range vs. Maximum Voltage Rating of Power MOSFETs

| Maximum Rated Drain-Source Voltage (V) | Minimum Ion Range (μm) |
|---|---|
| ≤ 100 | 30 |
| 100 to 250 | 40 |
| 250 to 400 | 80 |
| 400 to 1000 | 200 |

SEGR testing is usually done in a series of irradiations where the drain (or gate) voltage is increased in small steps. The highest "pass" voltage will be used to define failure. For example, if tests are done on a device with a 200 V rating in 10 volt steps, then the last test where the parts all worked properly will be defined as the failure point, not the next step where failure occurred.

The maximum voltage in circuit applications must be ≤ 75% of the highest pass voltage.

*Single-Event Burnout*

Single-event burnout requirements are essentially the same as for SEGR, with the exception that SEB can also occur in bipolar transistors. The signature of SEB is an increase in the drain current (for a power MOSFET), or the collector current (for a bipolar transistor).

*B. Design Verification*

As discussed earlier, the net impact of SEE effects depends on the specific design of circuits and systems. We can divide these effects into three general categories:

- Devices that are immune to SEE effects
- Devices that are affected by catastrophic SEE, where it is necessary to show that sufficient derating has been applied to avoid the effect
- Devices that are affected by recoverable SEE effects, where it is necessary to show that the specific design can tolerate the effect.

The last category is the one that requires the most effort.

*C. Circuit and System Hardening Methods*

A number of approaches can be used at the circuit and system level to mitigate recoverable SEE effects, and a few examples are illustrated below.

Various circuit and system mitigation approaches have been developed in order to overcome SEU issues in fielded space systems. Circuit mitigation methods include the use of clocked logic systems to reduce the time window where transients or short-duration state changes can affect performance." watchdog" timers that are used in simple circuits that will start auto-recovery methods if the expected response does not occur within the window of the timer, and duplication or triplication of critical circuit functions to detect abnormal behavior. There is also the "brute force" method of adding capacitors to slow down circuit response.

The technique that receives the most attention is error-detection-and-recovery (EDAC). EDAC uses an extended word length, relying on parity checking for error detection. Hamming codes are often used for EDAC. The commonly used implementations are

- "SECDED", single-error correction with correction of double-bit errors, requiring 32 data bits and 7 parity bits for a 32-bit effective word length, and
- "DECTED", which detects and corrects for both single-bit and double-bit errors, and detects (but does not correct) triple errors within a word. DECTED requires 64 data bits along with 15 parity bits, which imposes a much higher penalty compared to SECDED.

EDAC is not perfect, and errors may result if the event rate is too high. The rate of uncorrected errors, $E_{prop}$, that propagate when EDAC is implemented is approximately

$$E_{prop} = 0.5 \frac{T_{scrub}}{N_{EDAC}} U^2 \qquad (5)$$

where U is the upset error rate per device, $T_{scrub}$ is the time between successive "scrubs" of the memory array to correct for accumulated errors, and $N_{EDAC}$ is the number of words in the system. The number of uncorrected errors depends on the square of the upset rate, which is important because the upset rate can increase by several orders of magnitude during an intense solar flare.

Hamming error codes have been successfully applied in solid-state recorder in several space systems. For example, an older solid-state recorder used on the Clementine mission (lunar mapping) had an uncorrected error rate of about 130 errors per day, with a total memory size of about 2 Gbit [34]. The errors were caused by galactic cosmic rays, producing a very steady error rate. That mission operated for about six months, with completely effective performance of the recorder.

*D. Issues and Oversights*

Despite the concern about SEE effects, there are several cases where it was evident from system performance that SEE phenomena were causing effects in spacecraft that had not been anticipated. Two examples are shown below.

1. Resets in the solid-state power switches used on Cassini

The Cassini spacecraft uses approximately 400 highly efficient power switches that distribute power to various parts of the spacecraft. Once the spacecraft was launched, it became apparent that a small number of these switches were switching to different configurations, e.g., off-to-standby, or (in fewer cases) on-to-off. The problem was traced to SEE-induced transients in a

comparator, which was used in a non-clocked application that affected the switch whenever a transient with sufficient amplitude occurred. Fortunately the SET event rate was low enough that it has only a minor effect on the spacecraft performance. However, the low event rate is due to the extremely conservative way in which the comparator is used in the application, with a differential input voltage of 2.5 V. If a slightly lower value had been used – for example, 0.5 V – the event rate would have been several orders of magnitude higher, with far greater system impact.

The oversight occurred because SETs were not recognized as an important SEE effect during the time that the spacecraft was designed. Fig. 33 shows the number of events that occurred during nearly ten years of operation. The increased number of "on" to "off" trips after the spacecraft was inserted into orbit around Saturn is due to the larger number of switches that were placed in the "on" mode once the exploration mode began. The majority of the switches were in "off" or "standby" during the seven year cruise mode.

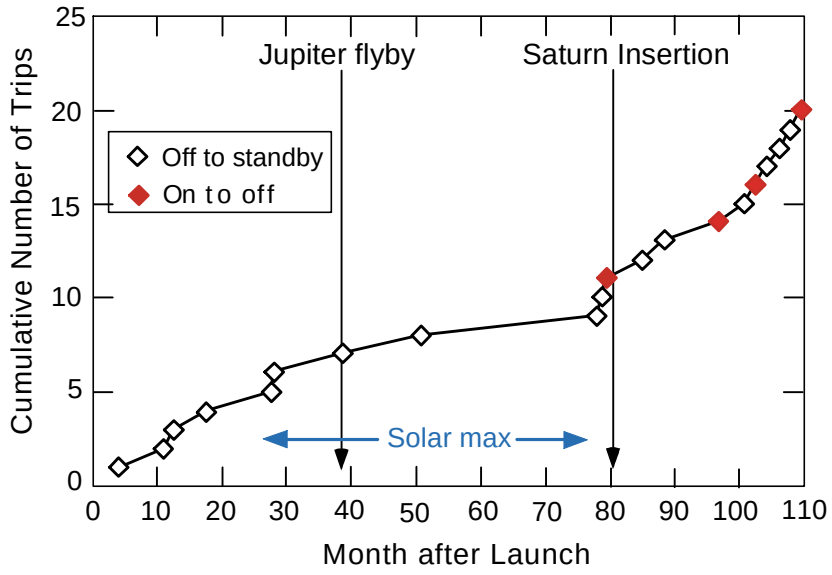


Fig. 33. Cumulative number of power switch trips for the 400 switch units on the Cassini spacecraft.

2. Upset rate in the Cassini solid-state recorder

The solid-state recorder used on Cassini incorporated EDAC to deal with the relatively high event rate that was expected because the dynamic memories (DRAMs) were highly sensitive to SEU effects. Approximately 200 errors occurred daily in the memory array from the cosmic ray background, but nearly all were successfully masked by the error correction algorithm. However, upon closer examination it was determined that many more errors were propagating through the EDAC than predicted from the expected number when the algorithm was applied. This result was checked several times, and although it remained low enough to allow the solid-state recorder to function adequately the error rate was about five orders of magnitude too high!

A careful investigation showed that the reason for this was an architectural flaw where more than one bit was used within a single memory chip. This allowed multiple upsets – which were a problem for older memories, and have become even more important as the size of memory cells has increased with scaling – to cause multiple errors to occur that could not be handled by the basic EDAC algorithm. Fig. 34 shows a diagram of the memory array, along with an example

of a case where two bits within a specific memory address were sufficiently close together to allow a multiple-bit upset to corrupt the memory.

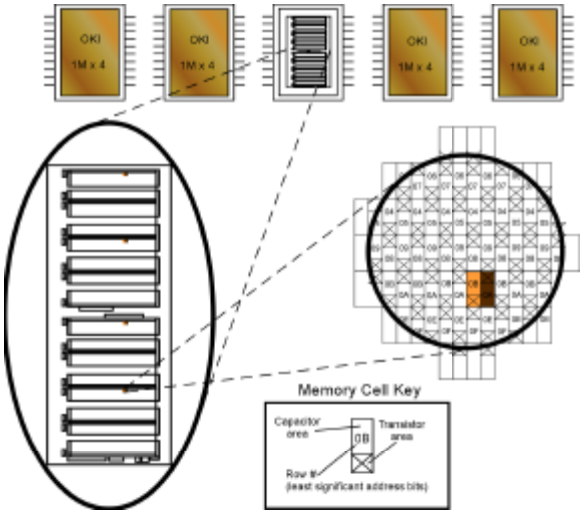


Fig. 34. Internal topology of the 4-Mb DRAM used on Cassini showing the location with the DRAM where multiple-bit upsets occurred that impacted the number of errors propagating through the EDAC.\

3. Error rate in hardened microprocessors.

Numerous JPL missions have used radiation-hardened microprocessors, and they have generally performed very well. However, as shown previously in Fig. 32 the low LET "tail" of the cross section cure results in a small but significant upset rate. About 20 such events have been observed in the JPL missions that have used those parts in deep space. In some cases the response signature is straightforward, but in other cases it requires a great deal of analysis of flight data to identify the problem. The point of this example is that even for hardened parts the system must be able to accommodate occasional upsets in hardened parts. For the most part the event rate is low enough to avoid problems, unless they occur at critical points in the mission (such as orbit insertion).

## IX. Summary and Conclusions

This document has discussed single-event upset and associated mechanisms, some of which are catastrophic. The complexity of modern devices has made it more difficult to deal with SEE effects, and their impact is strongly affected by the specific way in which they are used within a circuit or system.

Although we anticipate that most parts will be tested and qualified for SEE as part of the process of developing and implementing the Approved Parts and Materials List, it is still necessary for designers to understand the full impact of these effects on their designs. It should be clear from the discussion of the effects and the difficulties of radiation testing that it will be costly and involved to use parts that are not on the APML for the Europa program, and that the use of parts that are not on the APML is strongly discouraged.

Many of the parts used on Europa will not be immune to SEE effects. It is still possible to use them successfully as long as circuit and system designers understand the full impact of these effects. One of the challenges in developing the details for the APML will be to identify in a clear concise way how specific parts respond to SEE effects, and how circuit application details are related to them.

Fortunately the SEE environment of Europa is dominated by galactic cosmic rays, an environment which is nearly the same for most JPL missions. This allows us to make maximum use of experience with recent missions that use more advance part technologies.